

Display Elektronik GmbH

DATA SHEET

E-PAPER MODULE

DEE 152296A3-W 2.66“ **E-PAPER DISPLAY**

Product Specification

Ver.: 0

20.10.2023

| Version | Content | Date | Producer |
|----------------|----------------|-------------|-----------------|
| 0 | New Release | 20.10.2023 | JQ |
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1 General Description

DEE 152296A3-W is an Active Matrix Electrophoretic Display (Active Matrix E-Paper Display), with SPI-Interface and a reference system design. The 2.66" Active Area contains 152x296 pixels. The module is a TFT-Array driving electrophoretic display, with integrated circuits including gate buffer, source buffer, MCU interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2 Features

- ◆ 152×296 Pixels Display
- ◆ White Reflectance above 45%
- ◆ Contrast Ratio above 20:1
- ◆ Ultra Wide Viewing Angle
- ◆ Ultra Low Power Consumption
- ◆ Pure Reflective Mode
- ◆ Bi-Stable Display
- ◆ Landscape, Portrait Modes
- ◆ Ultra Low Current deep Sleep Mode
- ◆ On Chip Display RAM
- ◆ Serial Peripheral Interface available
- ◆ On-Chip Oscillator
- ◆ On-Chip Booster and Regulator Control for generating VCOM, Gate and Source Driving Voltage
- ◆ I²C Signal Master Interface to read external Temperature Sensor

3 Application

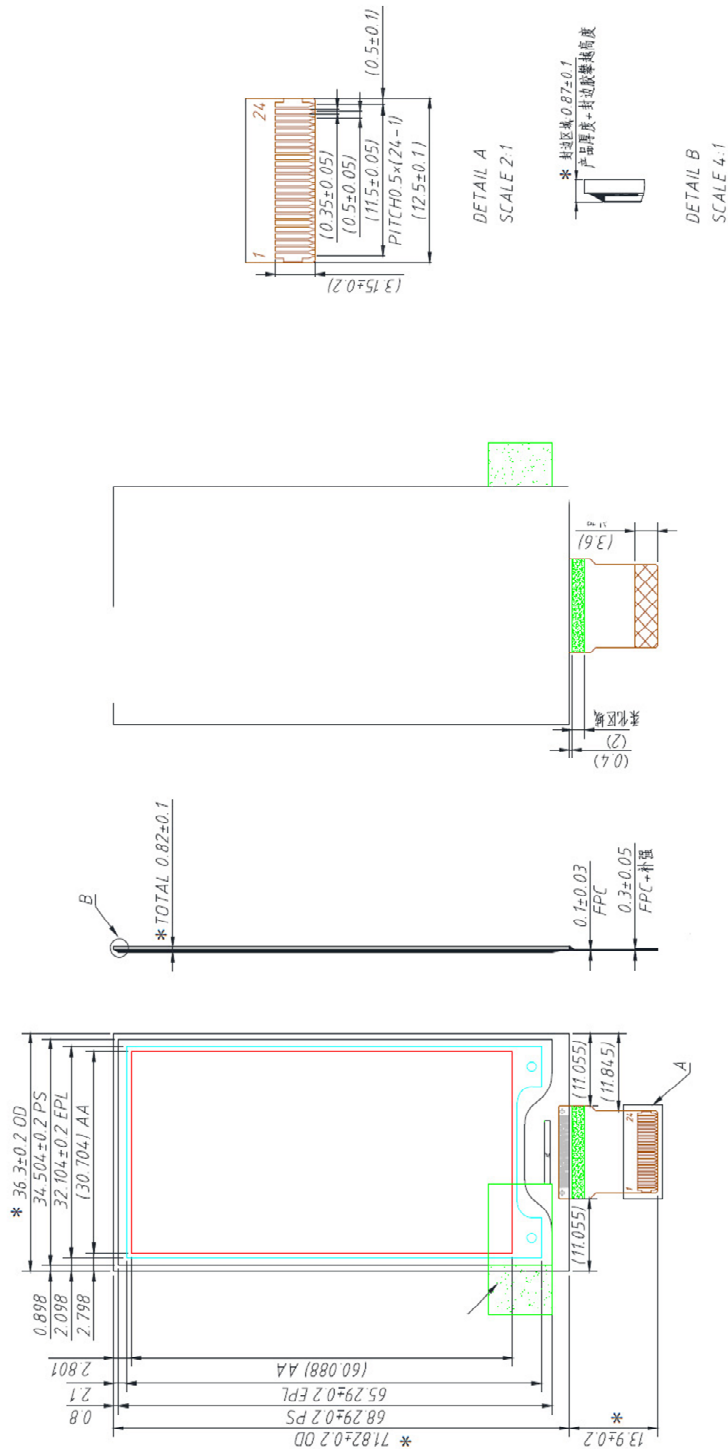
Electronic Shelf Label System or others.

4 Mechanical Specification

4.1 Dimension

| Parameter | Specifications | Unit |
|---------------------|-----------------------|-------------|
| Screen Size | 2.66 | Inch |
| Display Resolution | 152 x 296 | Pixel |
| Active Area | 30.704 x 60.088 | mm |
| Pixel Pitch | 0.202 x 0.203 | mm |
| Pixel Configuration | Rectangle | - |
| Outline Dimension | 36.30 x 71.80 x 0.82 | mm |
| Weight | ~ 4.6 | g |

4.2 Mechanical Drawing of EPD Module



NOTES:

4. Mark" * "for control DIM.
"1" DIM does not need to be measured.
标注 * "为管径尺寸, 1"里面尺寸不需要量。
5 Product thickness (THK) include: TFT+EPL+PS.
TFT+EPL+PS.
3 Material conform to the RoHS standard;
未指定公差: ± 0.20 ;
2 Unsperificed Tolerance ± 0.20 ;
显示模组为: 2.60寸;
1 TFT Display module 2.60" array for EPD;

5 Input / Output Pin Assignment

| No. | Name | I/O | Description | Remark |
|-----|-------|-----|---|----------|
| 1 | NC | / | Do not connect with other NC pins | - |
| 2 | GDR | O | N-Channel MOSFET Gate Drive Control | - |
| 3 | RESE | I | Current Sense Input for the Control Loop | - |
| 4 | NC | / | Do not connect with other NC pins | - |
| 5 | VDHR | C | Positive Source driving voltage 1 | - |
| 6 | TSCL | O | I ² C Interface to digital temperature sensor Clock pin | - |
| 7 | TSDA | I/O | I ² C Interface to digital temperature sensor Data pin | - |
| 8 | BS | I | Bus Interface selection pin | Note 5-4 |
| 9 | BUSYN | O | Busy state output pin | Note 5-3 |
| 10 | RSTN | I | Reset signal input. Active Low. | - |
| 11 | D/C | I | Data /Command control pin | Note 5-2 |
| 12 | CSB | I | Chip select input pin | Note 5-1 |
| 13 | SCL | I | Serial Clock pin (SPI) | - |
| 14 | SDA | I/O | Serial Data pin (SPI) | - |
| 15 | VDD | P | Power Supply for interface logic pins | - |
| 16 | VDD | P | Power Supply for the chip | - |
| 17 | VSS | P | Ground | - |
| 18 | VDDD | C | Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and VSS under all circumstances | - |
| 19 | VPP | P | Power Supply for OTP Programming | - |
| 20 | VSH | C | Positive Source driving voltage 2 | - |
| 21 | VGH | C | Positive Gate driving voltage | - |
| 22 | VSL | C | Negative Source driving voltage | - |
| 23 | VGL | C | Negative Gate driving voltage | - |
| 24 | VCOM | C | VCOM driving voltage | - |

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

Note 5-2: This pin is Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at D1 will be interpreted as data. When the pin is pulled LOW, the data at D1 will be interpreted as command.

Note 5-3: This pin is busy state output pin. When busy is Low, the operation of chip should not be interrupted, command should not be sent, e.g., the chip would put Busy pin Low when

- Outputting display waveform
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-4: Bus interface selection pin

| BS State | MCU Interface |
|----------|--|
| L | 4-lines serial peripheral interface(SPI) |
| H | 3- lines serial peripheral interface(SPI) - 9 bits SPI |

6 Electrical Characteristics

6.1 Absolute Maximum Rating

| Parameter | Symbol | Rating | Unit |
|----------------------|-----------|------------------------|------|
| Logic Supply Voltage | V_{dd} | -0.5 to +4.0 | V |
| Logic Input Voltage | V_{IN} | -0.5 to $V_{dd} + 0.5$ | V |
| Logic Output Voltage | V_{OUT} | -0.5 to $V_{dd} + 0.5$ | V |

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 Panel DC Characteristics

The following specifications apply for: $V_{SS}=0V$, $V_{DD}=3.0V$, $T_{OPR}=25^{\circ}C$.

| Parameter | Symbol | Condition | Applicable pin | Min. | Typ. | Max. | Unit |
|---------------------------|----------------|-------------------|----------------|--------------|------|--------------|------|
| Logic Supply Voltage | V_{dd} | - | VDD | 2.4 | 3.0 | 3.6 | V |
| High Level Input Voltage | V_{IH} | - | - | $0.8 V_{dd}$ | - | - | V |
| Low Level Input Voltage | V_{IL} | - | - | - | - | $0.2 V_{dd}$ | V |
| High Level Output Voltage | V_{OH} | $IOH = -100\mu A$ | - | $0.9 V_{dd}$ | - | - | V |
| Low Level Output Voltage | V_{OL} | $IOL = 100\mu A$ | - | - | - | $0.1 V_{dd}$ | V |
| OTP Program Voltage | V_{PP} | - | VPP | - | 8.25 | - | V |
| Typical Power Panel | P_{TYP} | - | - | - | 12 | 120 | mW |
| Deep Sleep Mode | P_{STPY} | - | - | - | 4.0 | - | uW |
| Typical Operating Current | I_{opr_VDD} | $V_{dd} = 3.0V$ - | - | - | 4.0 | 10 | mA |

| | | | | | | | |
|---------------------------------|------------------|--|-----|-----|----|------|-----|
| Sleep Mode Current | Islp_VDD | VDD=3.0V DC/DC OFF No clock No output load Ram data retain | VDD | - | 26 | -- | uA |
| Deep Sleep Mode Current | IdslpVDD | VDD=3.0V DC/DC OFF No clock No output load Ram data not retain | VDD | - | 1 | -- | uA |
| Operation Temperature Range | T _{OPR} | - | - | 0 | - | 50 | °C |
| Operation Illuminance Intensity | E | indoor only | - | - | - | 2000 | lux |
| Storage Temperature Range | T _{STG} | - | - | -25 | - | 60 | °C |
| Storage Relative Humidity | RHst | - | - | 30 | - | 60 | %RH |

Notes: 1. The typical power is measured with following transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Figure 10-2)

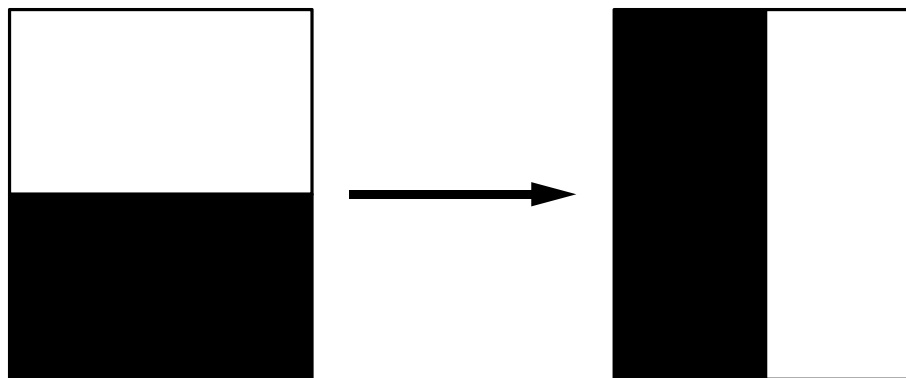


Figure 10-2 The typical Power Consumption measure Pattern

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by supplier.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

MCU interface consist of 2 data/command pins and 3 control pins. The pin assignment at different interface mode is summarized in Table 10-4-1. Different MCU mode can be set by hardware selection on BS pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

| Pin Name | Data/Connmand Interface | | Control Signal | | |
|---------------|-------------------------|------|----------------|-----|------|
| Bus interface | SDA | SCL | CSB | D/C | RSTN |
| 4-wire SPI | SDIN | SCLK | CSB | D/C | RSTN |
| 3-wire SPI | SDIN | SCLK | CSB | L | RSTN |

Table 10-4-1: MCU interface assignment under different bus interface mode

6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C, CSB. In 4-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

| Function | CSB | D/C | SCLK |
|---------------|-----|-----|------|
| Write command | L | L | ↑ |
| Write data | L | H | ↑ |

Note: ↑ stands for rising edge of signal

Table10-4-2: Control pins of 4-wire Serial interface

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

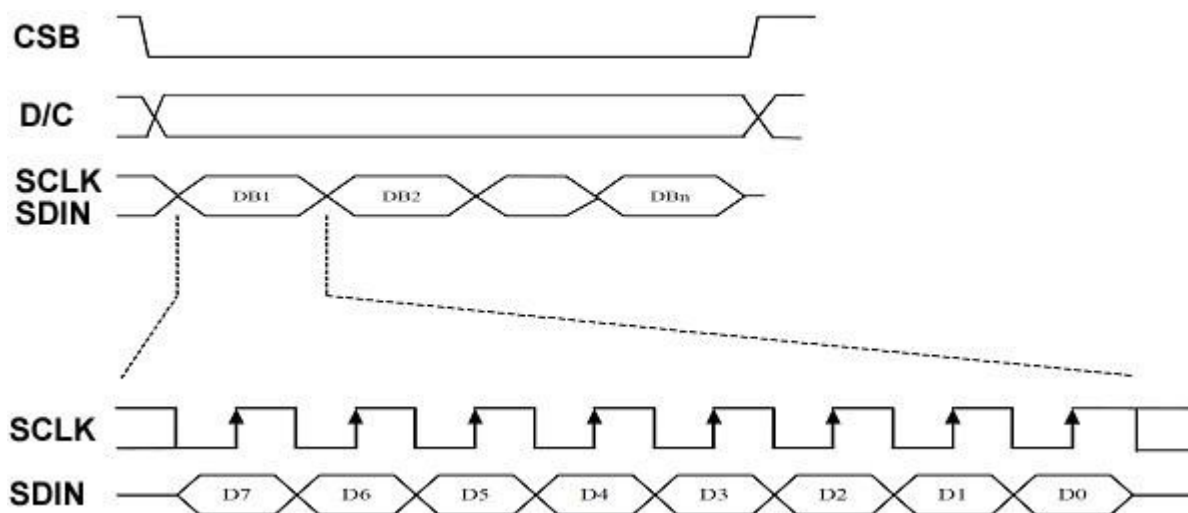


Figure 10-4-2: Write procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CSB. In 3-wire SPI mode, SCL acts as SCLK, SDA acts as SDIN.

The operation is similar to 4-wire serial interface while D/C pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C bit, D7 to D0 bit. The D/C bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C bit = 1) or the command register (D/C bit = 0).

Under serial mode, only write operations are allowed.

| Function | CSB | D/C | SCLK |
|---------------|-----|-----|------|
| Write command | L | Tie | ↑ |
| Write data | L | Tie | ↑ |

Note: ↑ stands for rising edge of signal

Table 10-4-3: Control pins of 3-wire Serial interface

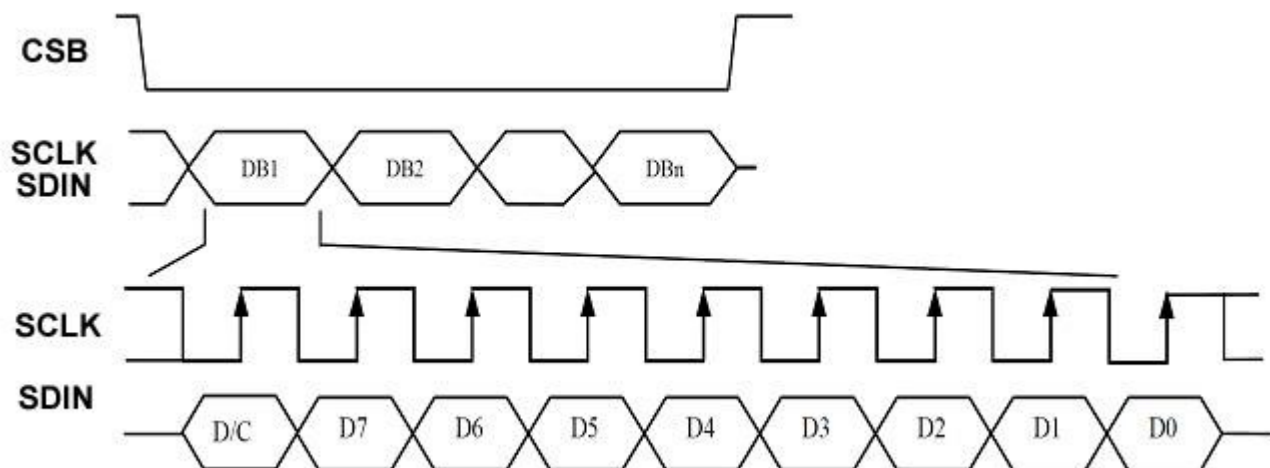


Figure 10-4-3: Write procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VDD =3.0V, T_{OPR} =25°C.

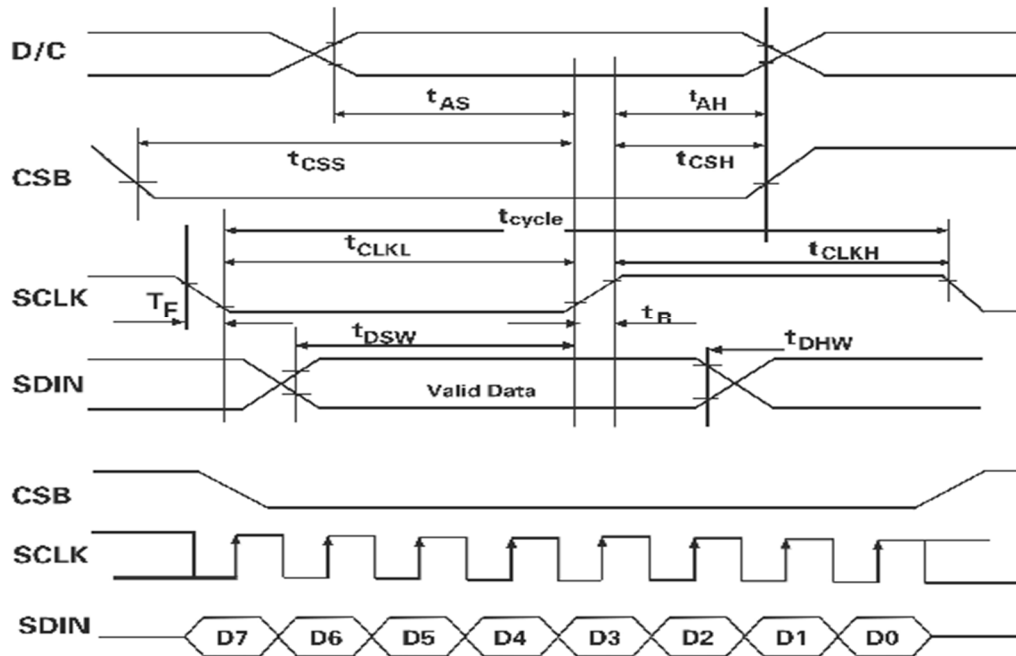


Figure 10-4-4: Serial interface characteristics

(V_{dd} - VSS = 2.4V to 3.3V, T_{OPR} = 25°C, CL=20pF)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------------------|------------------------|------|------|------|------|
| t _{cycle} | Clock Cycle Time | 250 | - | - | ns |
| t _{AS} | Address Setup Time | 150 | - | - | ns |
| t _{AH} | Address Hold Time | 150 | - | - | ns |
| t _{CSS} | Chip Select Setup Time | 120 | - | - | ns |
| t _{CSH} | Chip Select Hold Time | 60 | - | - | ns |
| t _{DSW} | Write Data Setup Time | 50 | - | - | ns |
| t _{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t _{CLKL} | Clock Low Time | 100 | - | - | ns |
| t _{CLKH} | Clock High Time | 100 | - | - | ns |
| t _R | Rise Time [20% ~ 80%] | - | - | 15 | ns |
| t _F | Fall Time [20% ~80%] | - | - | 15 | ns |

Table 10-4-4: Serial Interface Timing Characteristics

7 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

| Symbol | Parameter | Conditions | Values | | | Units | Notes |
|---------------------|--------------------|------------|--------|------|-----|-------|-------|
| | | | Min. | Typ. | Max | | |
| R | White Reflectivity | White | 45 | 48 | - | % | 11-1 |
| CR | Contrast Ratio | | 20:1 | 25:1 | - | - | 11-2 |
| T _{update} | Full Refresh | at +25°C | 500 | 750 | - | ms | 11-3 |
| | Partial Refresh | at +25°C | - | 250 | - | ms | |

Notes: 11-1. Luminance meter: Eye-One Pro Spectrophotometer.

11-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

11-3. Waveform provided by supplier is required.

Full refresh: The screen will flicker several times during the refresh process.

Partial refresh: The screen does not flicker during the refresh process.

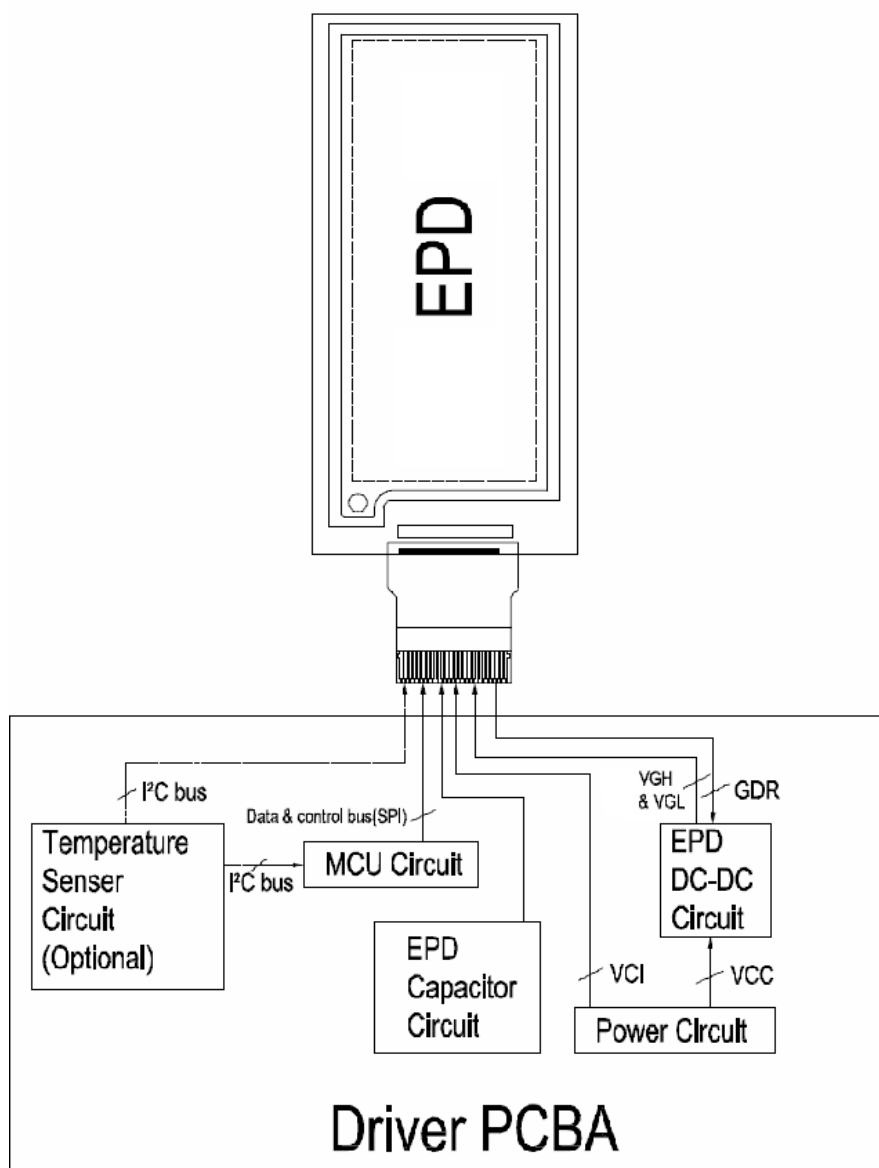
8 Handling, Safety, and Environment Requirements

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel
2. The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
3. Do not apply pressure to the EPD panel in order to prevent damaging it
4. Do not connect or disconnect the interface connector while the EPD panel is in operation
5. Do not stack the EPD panels / Modules.
6. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
7. Do not disassemble or reassemble the EPD panel
8. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet
9. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation
10. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
11. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package. Without sunlight, without condensation a temperature range of 15°C to 35°C, and humidity from 30%RH to 60%RH.

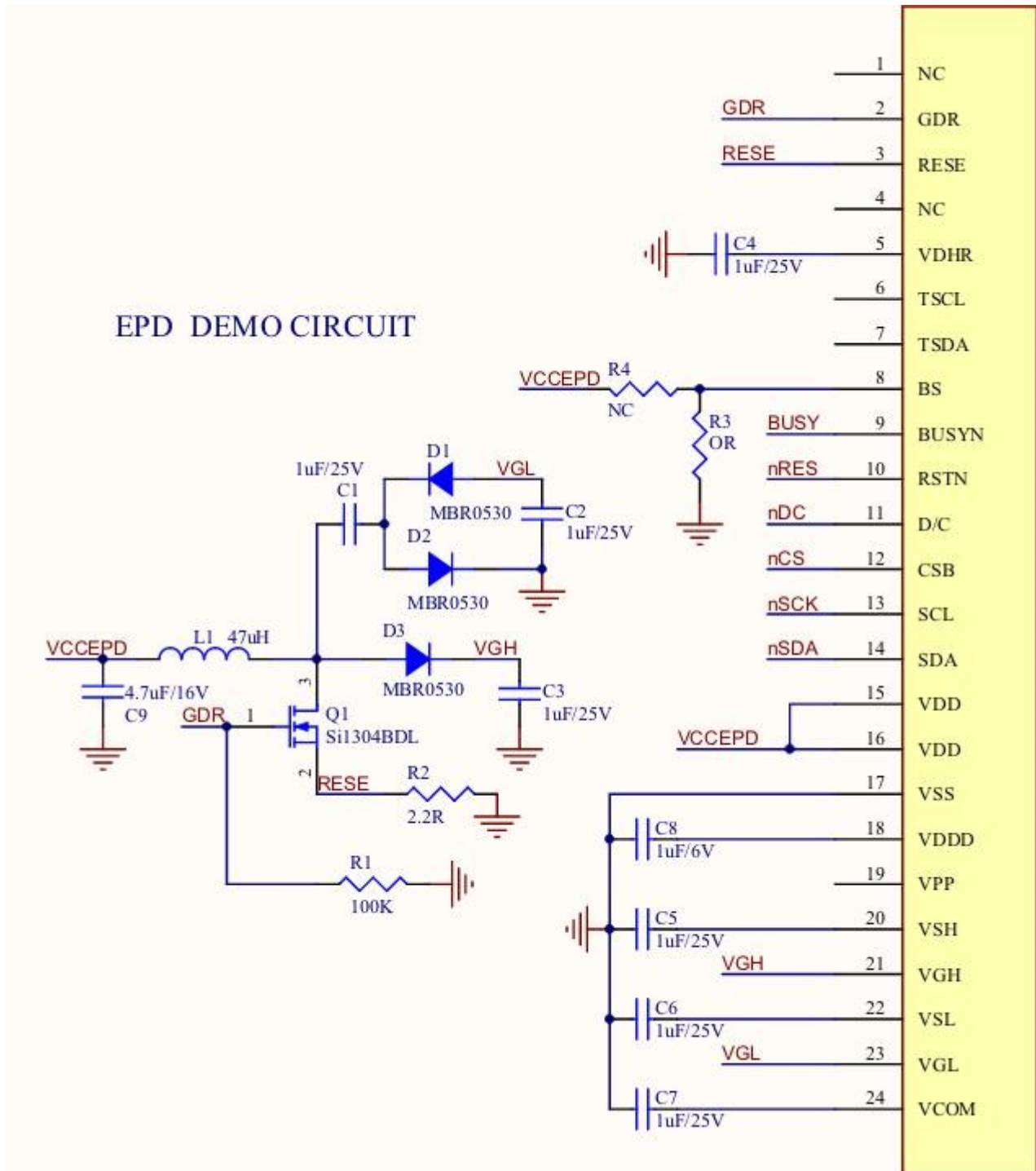
9 Reliability Test

| No. | Test | Condition | Method | Remark |
|-----|---|---|--------------------------|--|
| 1 | High-Temperature Operation | T = +50°C, RH = 30% for 240 hrs | IEC 60 068-2-2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 2 | Low-Temperature Operation | T = 0°C for 240 hrs | IEC 60 068-2-2Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 3 | High-Temperature Storage | T = +70°C, RH=23% for 240 hrs | IEC 60 068-2-2Bp | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 4 | Low-Temperature Storage | T = -25°C for 240 hrs | IEC 60 068-2-1Ab | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 5 | High-Temperature, High-Humidity Operation | T = +40°C, RH = 90% for 168 hrs | IEC 60 068-2-3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 6 | High Temperature, High-Humidity Storage | T = +60°C, RH=80% for 240hrs | IEC 60 068-2-3CA | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 7 | Thermal Shock | 1 cycle:[-25°C 30min]→[+70 °C 30 min] : 100 cycles | IEC 60 068-2-14 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 8 | Package Vibration | 1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 9 | Package Drop Impact | Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3edges, 6 faces One drop for each | Full packed for shipment | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |
| 10 | Electrostatic Effect (non-operating) | Machine model +/- 250V, 0Ω, 200pF | IEC 62179, IEC 62180 | At the end of the test, electrical, mechanical, and optical specifications shall be satisfied. |

10 Block Diagram



11 Typical Application Circuit with SPI Interface



References for component selection as below:

| Components | Value/Type | Requirements |
|------------|---------------|--|
| C1-C8 | 1uF | Dielectric: X5R/X7R, Rated Voltage: 25V |
| C9 | 4.7uF | Dielectric: X5R/X7R, Rated Voltage: 25V |
| D1-D3 | diode | MBR0530 1.reverse DC \geq 30V 2.Io \geq 500mA 3.Forward \leq 430mV |
| R1 | 100K Ω | 1% |
| R2 | 2.2 Ω | 1% |
| Q1 | NMOS | Si1304BDL 1.Drain Source breakdown voltage \geq 30V 2.Vgs(Vth)=0.9V (TYP)) ,1.3V(Max) 3. Rds on \leq 2.1 Ω @ Vgs=2.5V |
| L1 | 47uH | CDRH2D18/LDNP-470NC Io=500(Max) |

12 Inspection Standard

12.1 Appearances Inspection Standard

12.1.1 Appearances Specification

This appearance inspection shall be applied to segment EPD modules.

12.1.2 Inspection Conditions

Viewing Angle: $\alpha = \pm 45^\circ$

Viewing Distance: 30cm \pm 10cm

Ambient Luminance: 700~1000 Lux.

Supply Voltage: Typical value described on the Electrical Characteristics

Environment Ambient Temperature: 20°C~25°C

Environment Ambient Humidity: 40~70%RH

ESD should be controlled within $\pm 200V$

12.1.3 Inspection Level: Level II

Sampling table: GB/T 2828.1-2012 II, unless otherwise agreed in writing.

12.1.4 Acceptance Quality Level (AQL)

Major Defect: 0.65 , Minor Defect: 1.5

12.1.5 Classification of Defects

Defects are classified as either a major or a minor defect defined as below.

Major Defect :It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.

Minor Defect :It is a defect that will not result in functioning problem with deviation classified.

12.3 Quality Criteria

12.3.1 Zone Definitions

A Zone: EPD Active Area (not including border)

B Zone: Out of Active Area

12.3.2 Appearances Criteria

As shown in the tables below. If any other items, standard values or applicable zones are required to be defined, a written agreement shall be signed, and otherwise a limited sample shall be made for reference.

Major Defects:

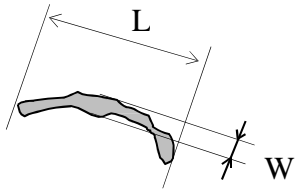
| Item | Description | Classification |
|------------------|---|----------------|
| No Display | No display shown on screen due to malfunction | Major |
| Line Missing | Line missing | Major |
| Abnormal Display | Unusual pattern or function displayed | Major |
| TFT Broken | TFT broken by external force | Major |

Minor Defects:

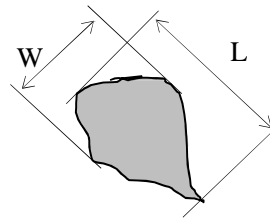
| Item | | Criteria | Specific Zone | |
|-------------|---|---|---------------|--------|
| Name | Description | | A Zone | B Zone |
| Dot defect | Spot/ Air bubble/ Foreign material in dot shape | D≤0.30mm | Ignore | Ignore |
| | | 0.30mm<D≤0.50mm | ≤5 | |
| | | D>0.50mm | 0 | |
| Line defect | Scratch on top surface/ Foreign material in line or spiral shape | L≤1.0 mm , W≤0.15mm | Ignore | Ignore |
| | | 1.0mm<L≤5.0mm & 0.15mm<W≤0.5mm | ≤4 | |
| | | L>5.0mm or W>0.5mm | 0 | |
| Chipping | Corner chip | Not affect the display, not have diffuse or comminuted cracks | | |
| | Edge chip | | | |
| Curl | Curl for Panel | ≤1.0 mm | | |

Remarks:

Definitions of “line” and “dot”:

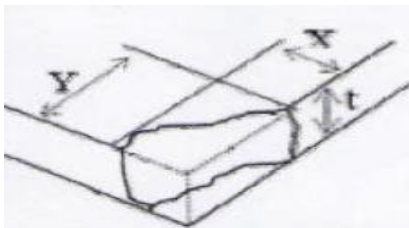


a. Line

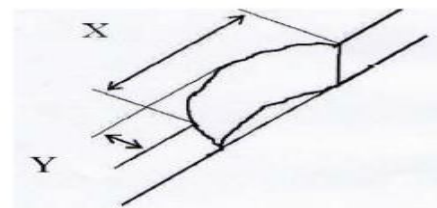


b. Dot

When $L \leq 0.5\text{mm}$ or $L < 4W$, defined as a dot. Definitions of “Chipping”:



c. Corner chip



d. Edge chip