Display Elektronik GmbH

DATA SHEET

TFT- MODULE

DEM 7201280B VRH

5,5” refl. TFT

Product Specification Ver.: 3

18.02.2024

Revision History

Revision	Date	Originator	Detail	Remarks
0	23.12.2023	LQ	Initial Release	-
1	04.01.2024	LQ	Modify Module Outline Size Modify Outline Drawing(B)	P4 P24
2	29.01.2024	LQ	Modify Interface Pins Description Modify Outline Drawing	P10 P24
3	18.02.2024	DFG	Add Weight Add Current Consumption Modify Outline Drawing	P4 P5 P24

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1. General Description

The specification is a reflective type color active matrix liquid crystal display (LCD) which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT-LCD panel, driver ICs.

2. Module Parameter

Features	Details	Unit
Display Size(Diagonal)	5.5”	
Display Mode	Reflective /Normally white	
Resolution	720 RGB x 1280	Pixels
View Direction	FULL VIEW	Best Image
Module Outline	70.64 x 126.44 x 0.85 (Note1)	mm
Active Area	68.04 x 120.96	mm
Pixel Size	0.945 x 0.945	mm
Pixel Arrangement	RGB Vertical Stripe	
Display Colors	16.7M	
Interface	MIPI interface	
With or without touch panel	Without	
Driver IC	ILI9881C	-
Operating Temperature	-20～70	ºC
Storage Temperature	-30～80	ºC
Weight	16	g

Note 1: Exclusive hooks, posts, FFC/FPC tail etc.

3. Absolute Maximum Ratings

GND=0V, Ta=25ºC

Item	Symbol	Min.	Max.	Unit
Supply Voltage	VCI	-0.3	7.0	V
	IOVCC	-0.3	3.8	V
Storage temperature	T_{STG}	-30	+80	ºC
Operating temperature	T_{OP}	-20	+70	ºC

Note 1: If Ta below 50ºC, the maximal humidity is 90%RH, if Ta over 50ºC, absolute humidity should be less than 60%RH.

Note 2: The response time will be extremely slow when the operating temperature is around -10℃, and the back ground will become darker at high temperature operating.

4. DC Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage		VCI	2.5	2.8	6.6	V
		IOVCC	1.65	1.8	3.6	V
Logic High level input voltage		V_{IH}	0.7* IOVCC	-	IOVCC	mV
Logic Low level input voltage		V_{IL}	-0.3	-	0.3* IOVCC	mV
Logic High level Output voltage		V_{OH}	0.8* IOVCC	-	IOVCC	mV
Logic Low level Output voltage		V_{OL}	0	-	0.2* IOVCC	mV
Current Consumption All black	Logic	I_{CI+} I_{IO}	-	16	-	µA
	Analog					

5. Optical Characteristics

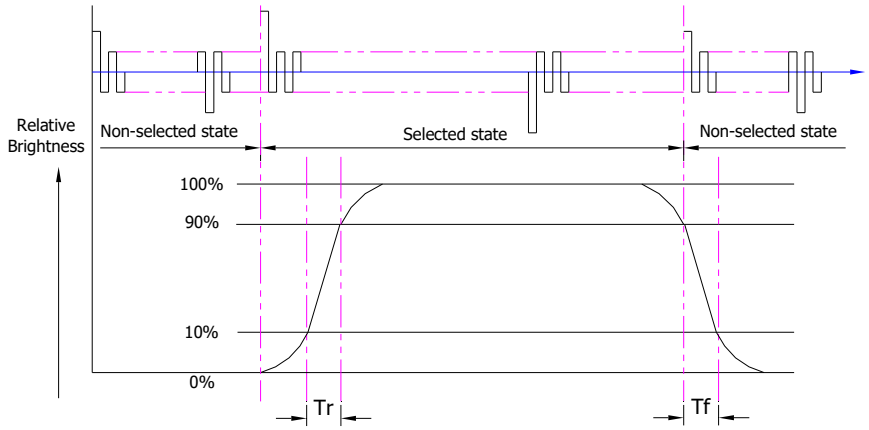
5.1. Optical Characteristics

Ta=25ºC,VCI=2.8V

Item		Symbol	Condition	Specification			Unit
				Min.	Typ.	Max.	
Contrast ratio(See 5.3)		CR	Normally viewing angle θX = φY =0º	-	15	-	-
Response time (See 5.2)		TR+TF		-	5	7	ms
Chromaticity Reflective (See 5.5)	Red	XR		-	-	-	-
		YR		-	-	-	-
	Green	XG		-	-	-	-
		YG		-	-	-	-
	Blue	XB		-	-	-	-
		YB		-	-	-	-
	White	XW		-	-	-	-
		YW		-	-	-	-
Viewing Angle (See 5.4)	Horizontal	θX+	Center CR≥10	-	60	-	Deg.
		θX-		-	60	-	
	Vertical	φY+		-	60	-	
		φY-		-	60	-	
NTSC Ratio(Gamut)				-	7	-	%

5.2. Definition of Response Time

5.2.1. Normally Black Type (Negative)

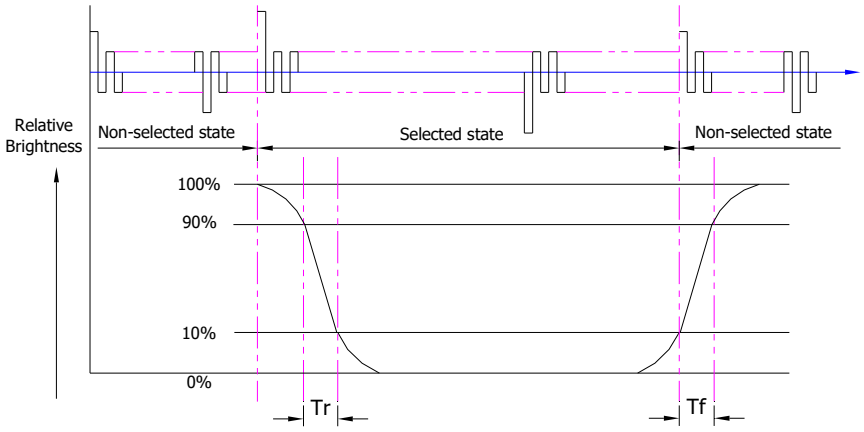


Tr is the time it takes to change form non-selected stage with relative luminance 10% to selected state with relative luminance 90%;

Tf is the time it takes to change from selected state with relative luminance 90% to non-selected state with relative luminance 10%.

Note: Measuring machine: LCD-5100

5.2.2. Normally White Type (Positive)



Tr is the time it takes to change form non-selected stage with relative luminance 90% to selected state with relative luminance 10%;

Tf is the time it takes to change from selected state with relative luminance 10% to non-selected state with relative luminance 90%;

Note: Measuring machine: LCD-5100 or EQUI

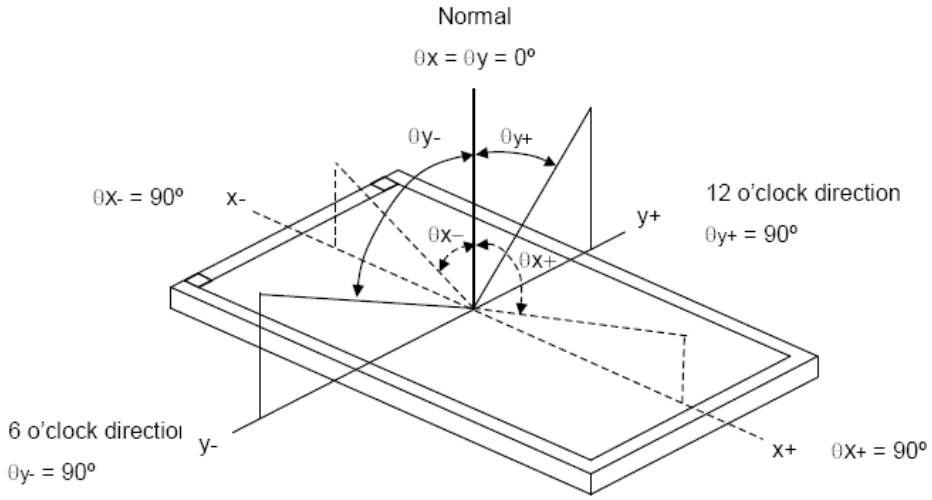
5.3. Definition of Contrast Ratio

Contrast is measured perpendicular to display surface in reflective and transmissive mode. The measurement condition is:

Measuring Equipment	Eldim or Equivalent
Measuring Point Diameter	3mm//1mm
Measuring Point Location	Active Area centre point
Test pattern	A: All Pixels white
	B: All Pixel black
Contrast setting	Maximum

Definitions: CR (Contrast) = Luminance of White Pixel / Luminance of Black Pixel

5.4. Definition of Viewing Angles



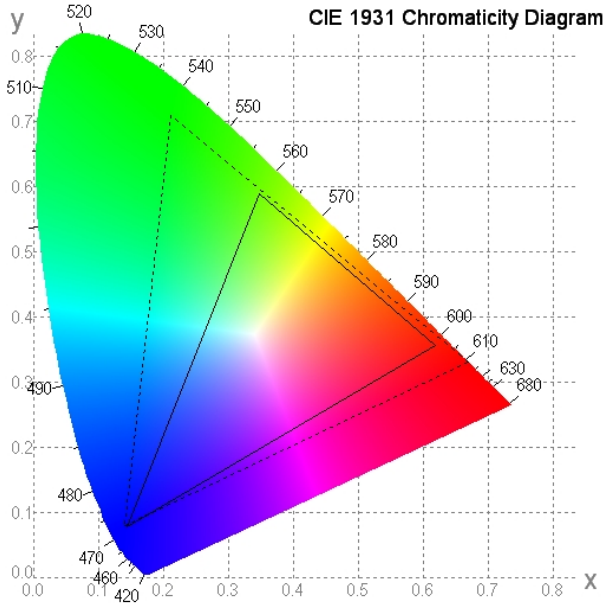
Measuring machine: LCD-5100 or EQUI

5.5. Definition of Color Appearance

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)



5.6. Definition of Surface Luminance, Uniformity and Transmittance

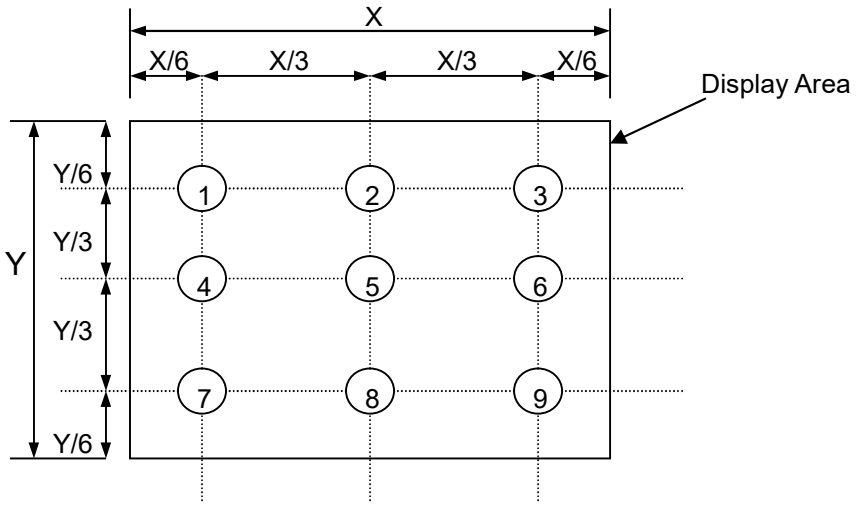
Using the Reflective mode measurement approach, measure the white screen luminance of the display panel and backlight.

5.6.1. Surface Luminance: L_V = average (L_{P1}:L_{P9})

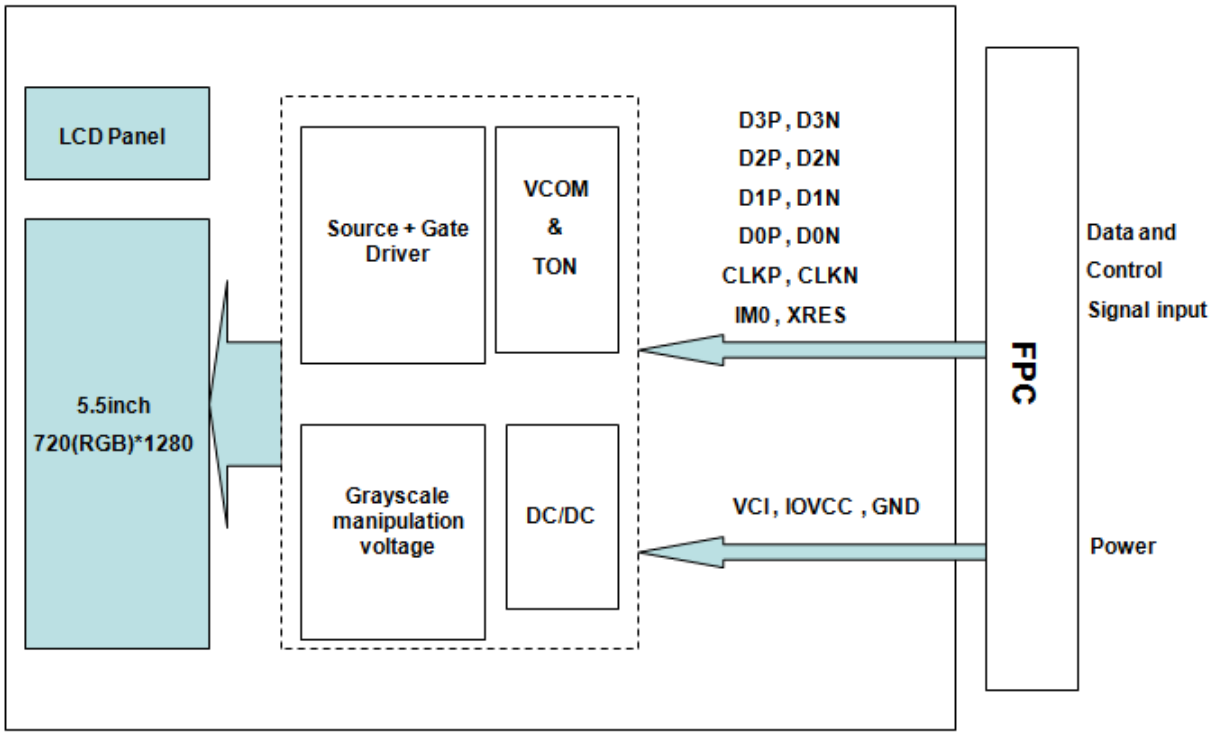
5.6.2. Uniformity = Minimal (L_{P1}:L_{P9}) / Maximal (L_{P1}:L_{P9}) * 100%

5.6.3. Transmittance = L_V on LCD / L_V on Backlight * 100%

Note: Measuring machine: BM-7



6. Block Diagram and Power Supply



7. Interface Pins Definition

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th><th>Remark</th></tr>
<tr><td>1</td><td>MTP_PWR</td><td>Input power for OTP programming. MTP_PWR=8.5V
When not under programming, let MTP_PWR float or connect to ground.</td><td></td></tr>
<tr><td>2</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>3</td><td>D3N</td><td>MIPI data Input</td><td></td></tr>
<tr><td>4</td><td>D3P</td><td>MIPI data Input</td><td></td></tr>
<tr><td>5</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>6</td><td>D2N</td><td>MIPI data Input</td><td></td></tr>
<tr><td>7</td><td>D2P</td><td>MIPI data Input</td><td></td></tr>
<tr><td>8</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>9</td><td>D1N</td><td>MIPI data Input</td><td></td></tr>
<tr><td>10</td><td>D1P</td><td>MIPI data Input</td><td></td></tr>
<tr><td>11</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>12</td><td>D0N</td><td>MIPI data Input</td><td></td></tr>
<tr><td>13</td><td>D0P</td><td>MIPI data Input</td><td></td></tr>
<tr><td>14</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>15</td><td>CLKP</td><td>MIPI clock Input</td><td></td></tr>
<tr><td>16</td><td>CLKN</td><td>MIPI clock Input</td><td></td></tr>
<tr><td>17</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>18</td><td>NC</td><td>No connection</td><td></td></tr>
<tr><td>19</td><td>NC</td><td>No connection</td><td></td></tr>
<tr><td>20</td><td>NC</td><td>No connection</td><td></td></tr>
<tr><td>21</td><td>IM0</td><td>Used to configure lane sequence and polarity
<table>
<tr><th colspan="3">External Pad Set</th><th colspan="5">Configuration of MIPI Lane</th></tr>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>D0P/N Pin</th><th>D1P/N Pin</th><th>CLKP/N Pin</th><th>D2P/N Pin</th><th>D3P/N Pin</th></tr>
<tr><td>0</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr>
</table></td><td></td></tr>
<tr><td>22</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>23</td><td>XRES</td><td>The external reset input.</td><td></td></tr>
<tr><td>24</td><td>LEDPWM</td><td>LCD backlight control PWM output pin.
Leave the pin open when not in use.</td><td></td></tr>
<tr><td>25</td><td>VCI</td><td>Power supply for analog circuit</td><td></td></tr>
<tr><td>26</td><td>IOVCC</td><td>Power supply for I/O circuit</td><td></td></tr>
<tr><td>27</td><td>NC</td><td>No connection</td><td></td></tr>
<tr><td>28</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>29</td><td>NC(LEDA)</td><td>No connection</td><td></td></tr>
<tr><td>30</td><td>NC(LEDK)</td><td>No connection</td><td></td></tr>
</table>

8. AC Characteristics

8.1. DSI Timing Characteristics

(1)

High Speed Mode – Clock Channel Timing

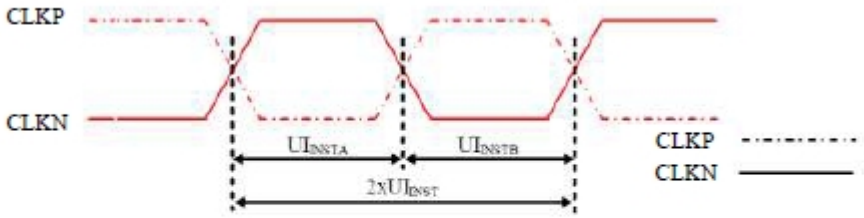


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	*Note 2*	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	*Note 2*	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

(2)

High Speed Mode – Data Clock Channel Timing

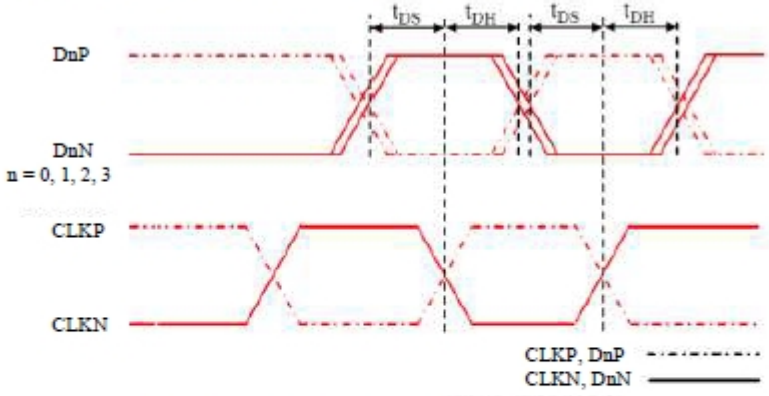


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

(3)

High Speed Mode – Rising and Falling Timings

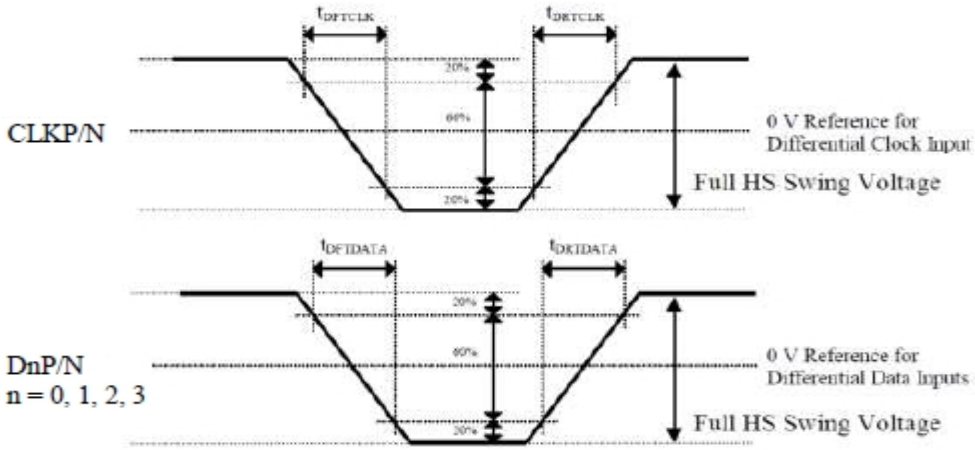


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

(4)

Data Lanes from Low Power Mode to High Speed Mode

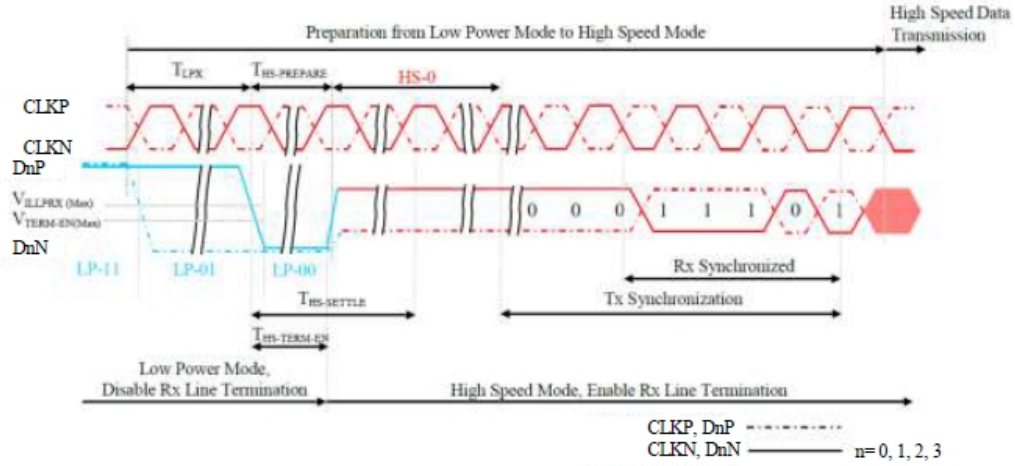


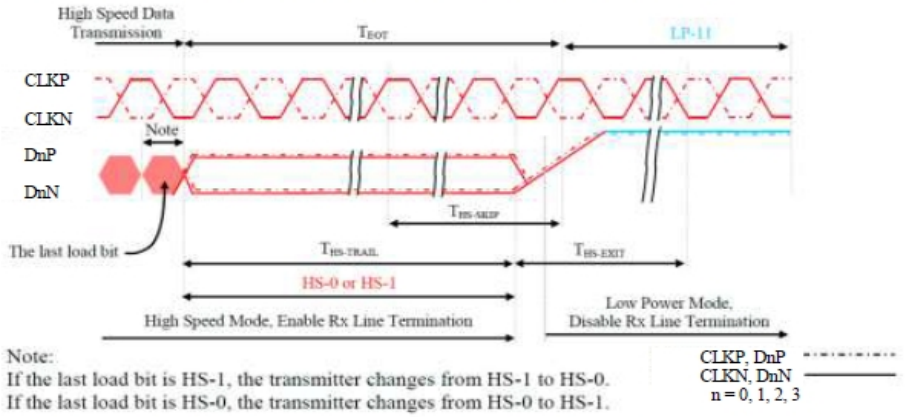
Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

(5)

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

(6)

DSI Clock Burst – High Speed Mode to/from Low Power Mode

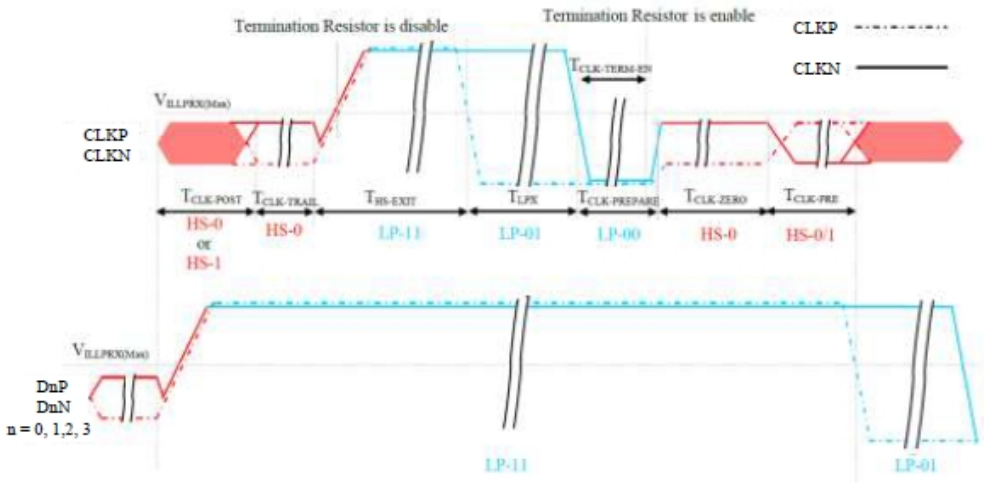
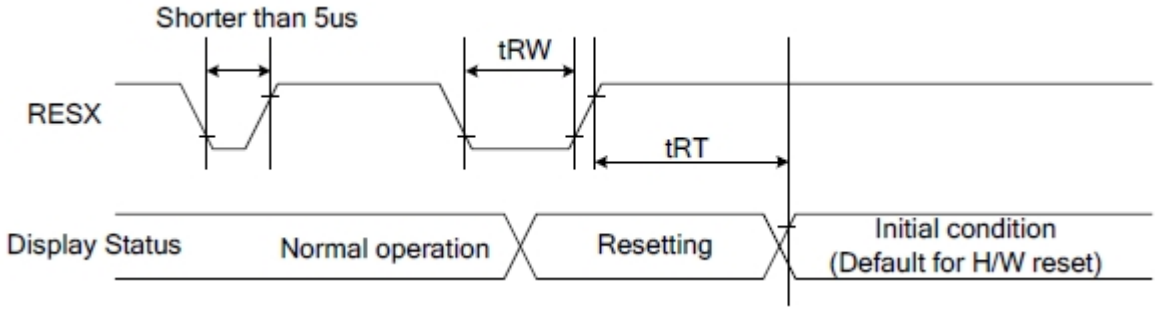


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

8.2. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

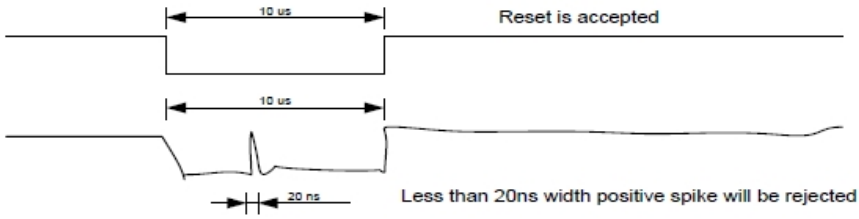
Notes:

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

9. Quality Assurance

9.1. Purpose

This standard for Quality Assurance assures the quality of LCD module products supplied to customer.

9.2. Standard for Quality Test

9.2.1. Sampling Plan:

GB2828.1-2012

Single sampling, general inspection level II

9.2.2. Sampling Criteria:

Visual inspection: AQL 1.5

Electrical functional: AQL 0.65.

9.2.3. Reliability Test:

Detailed requirement refer to Reliability Test Specification.

9.3. Nonconforming Analysis & Disposition

9.3.1. Nonconforming analysis:

9.3.1.1. Customer should provide overall information of non-conforming sample for their complaints.

9.3.1.2. After receipt of detailed information from customer, the analysis of nonconforming parts usually should be finished in one week.

9.3.1.3. If cannot finish the analysis on time, customer will be notified with the progress status.

9.3.2. Disposition of nonconforming:

9.3.2.1. Non-conforming product over PPM level will be replaced.

9.3.2.2. The cause of non-conformance will be analyzed. Corrective action will be discussed and implemented.

9.4. Agreement Items

Shall negotiate with customer if the following situation occurs:

9.4.1. There is any discrepancy in standard of quality assurance.

9.4.2. Additional requirement to be added in product specification.

9.4.3. Any other special problem.

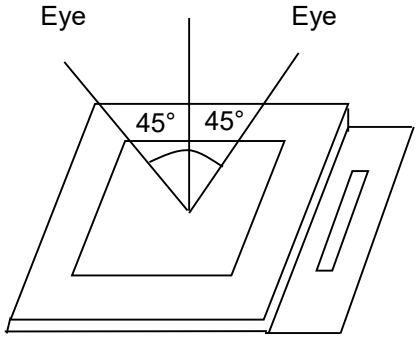
9.5. Standard of the Product Visual Inspection

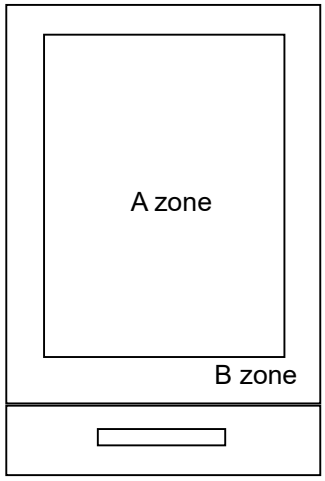
9.5.1. Appearance inspection:

9.5.1.1. The inspection must be under illumination about 1000 – 1500 lx, and the distance of view must be at 30cm ± 2cm.

9.5.1.2. The viewing angle should be 45° from the vertical line without reflection light or follows customer's viewing angle specifications.

9.5.1.3. Definition of area: A Zone: Active Area, B Zone: Viewing Area,



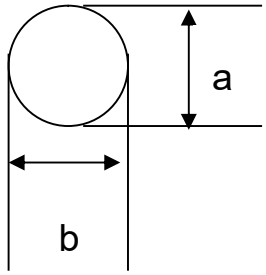


9.5.2. Basic principle:

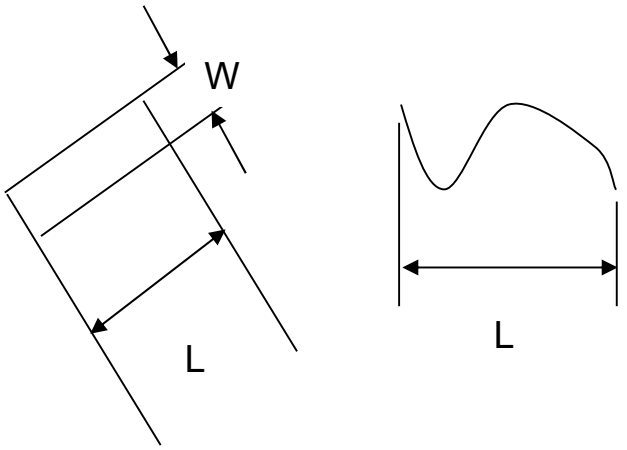
9.5.2.1. A set of sample to indicate the limit of acceptable quality level must be discussed by both us and customer when there is any dispute happened.

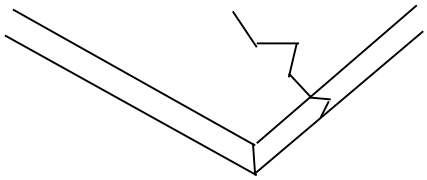
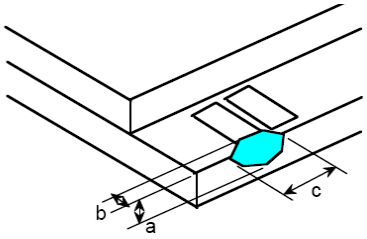
9.5.2.2. New item must be added on time when it is necessary.

9.6. Inspection Specification

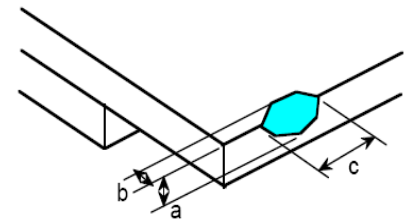
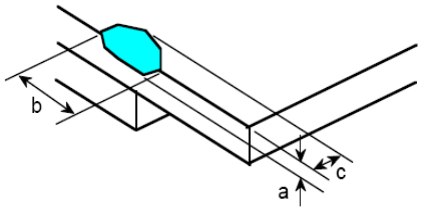
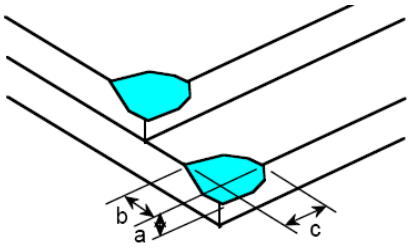
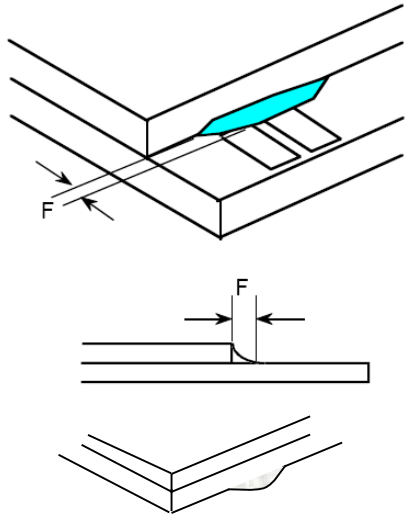
<table>
<tr><th>No.</th><th>Item</th><th>Criteria (Unit: mm)</th></tr>
<tr><td>01</td><td>Black / White spot
Foreign material
(Round type)
Pinholes
Stain
Particles inside cell. (Minor defect)</td><td>


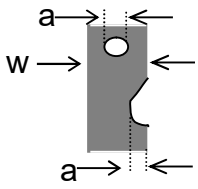
<table>
<tr><th>Area / Size</th><th>Acc. Qty</th></tr>
<tr><td>φ≤0.20</td><td>Ignore</td></tr>
<tr><td>0.20<φ≤0.50</td><td>N≤3</td></tr>
<tr><td>0.50<φ</td><td>0</td></tr>
</table>
φ= (a + b) /2
Distance between 2 defects should more than 3mm apart.
</td></tr>
<tr><td>02</td><td>Electrical Defect
(Minor defect)</td><td>
<table>
<tr><th></th><th>Display Area</th><th>Total</th><th></th></tr>
<tr><td>Bright dot</td><td>N⩽2</td><td>N⩽2</td><td rowspan="3">Note1</td></tr>
<tr><td>Dark dot</td><td>N⩽4</td><td>N⩽4</td></tr>
<tr><td>Total dot</td><td>N⩽4</td><td>N⩽4</td></tr>
<tr><td>Mura</td><td colspan="2">Not visible through 5% ND filters.</td><td>Note 2</td></tr>
</table>
Remark:
1. Bright dot caused by scratch and foreign object accords to item 1.
</td></tr>
</table>

<table>
<tr>
<td>03</td>
<td>Black and White line
Scratch
Foreign material
(Line type)
(Minor defect)</td>
<td>


<table>
<tr><th>Length</th><th>Width</th><th>Acc. Qty</th></tr>
<tr><td>/</td><td>W ≦ 0.03</td><td>Ignore</td></tr>
<tr><td>L ≦ 2.5</td><td>0.03 ＜ W ≦ 0.05</td><td>3</td></tr>
<tr><td>L ≦ 2.5</td><td>0.05 ＜ W ≦ 0.10</td><td>2</td></tr>
<tr><td>/</td><td>0.1 ＜ W</td><td>0</td></tr>
<tr><td colspan="2">Total</td><td>3</td></tr>
</table>
Distance between 2 defects should more than 3mm apart. Scratches not viewable through the back of the display are acceptable.
</td>
</tr>
<tr>
<td>04</td>
<td>Glass Crack
(Minor defect)</td>
<td>

Crack is potential to enlarge, any type is not allowed.
</td>
</tr>
<tr>
<td>05</td>
<td>Glass Chipping Pad Area:
(Minor defect)


</td>
<td>
<table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>3</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table>
</td>
</tr>
</table>

<table>
<tr>
<td>06</td>
<td>Glass Chipping Rear of Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>07</td>
<td>Glass Chipping Except Pad Area:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c > 3.0, b< 1.0</td><td>1</td></tr>
<tr><td>c< 3.0, b< 1.0</td><td>2</td></tr>
<tr><td>c< 3.0, b< 0.5</td><td>4</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>08</td>
<td>Glass Corner Chipping:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length and Width</th><th>Acc. Qty</th></tr>
<tr><td>c < 3.0, b< 3.0</td><td>Ignore</td></tr>
<tr><td colspan="2">a<Glass Thickness</td></tr>
</table></td>
</tr>
<tr>
<td>09</td>
<td>Glass Burr:
(Minor defect)
 
</td>
<td><table>
<tr><th>Length</th><th>Acc. Qty</th></tr>
<tr><td>F < 1.0</td><td>Ignore</td></tr>
</table>
Glass burr don’t affect assemble and module dimension.</td>
</tr>
</table>

<table>
<tr><td>10</td><td>FPC Defect:
(Minor defect)
 
</td><td>10.1 Dent, pinhole width a<w/3.
(w: circuitry width.)
10.2 Open circuit is unacceptable.
10.3 No oxidation, contamination and distortion.</td></tr>
<tr><td>11</td><td>Bubble on Polarizer
(Minor defect)</td><td><table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>12</td><td>Dent on Polarizer
(Minor defect)</td><td><table><tr><th>Diameter</th><th>Acc. Qty</th></tr><tr><td>φ≤0.20</td><td>Ignore</td></tr><tr><td>0.20 <φ≤0.30</td><td>4</td></tr><tr><td>0.30 <φ≤0.50</td><td>1</td></tr><tr><td>0.50 < φ</td><td>None</td></tr></table></td></tr>
<tr><td>13</td><td>Bezel</td><td>13.1 No rust, distortion on the Bezel.
13.2 No visible fingerprints, stains or other contamination.</td></tr>
<tr><td>14</td><td>PCB</td><td>14.1 No distortion or contamination on PCB terminals.
14.2 All components on PCB must same as documented on the BOM/component layout.
14.3 Follow IPC-A-600F.</td></tr>
<tr><td>15</td><td>Soldering</td><td>Follow IPC-A-610C standard</td></tr>
<tr><td>16</td><td>Electrical Defect
(Major defect)</td><td>The below defects must be rejected.
16.1 Missing vertical / horizontal segment,
16.2 Abnormal Display.
16.3 No function or no display.
16.4 Current exceeds product specifications.
16.5 LCD viewing angle defect.
16.6 No Backlight.
16.7 Dark Backlight.
16.8 Touch Panel no function.</td></tr>
</table>

Remark: LCD Panel Broken shall be rejected. Defect out of LCD viewing area is acceptable.

9.7. Classification of Defects

9.7.1. Visual defects (Except no / wrong label) are treated as minor defect and electrical defect is major.

9.7.2. Two minor defects are equal to one major in lot sampling inspection.

9.8. Identification/marking criteria

Any unit with illegible / wrong /double or no marking/ label shall be rejected.

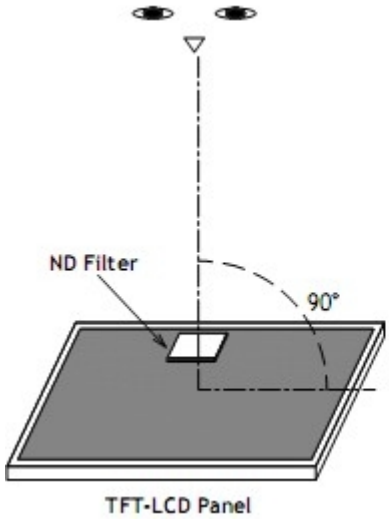
9.9. Packing

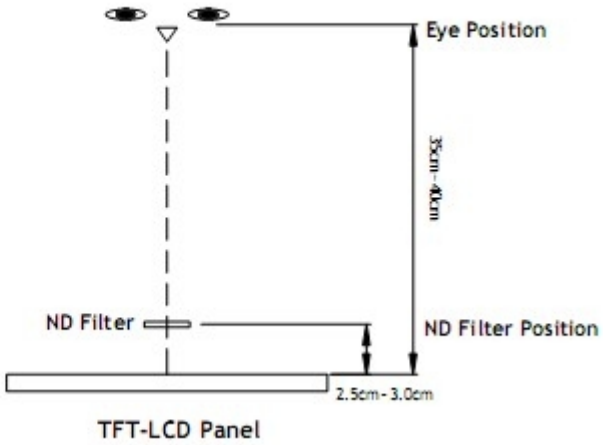
9.9.1. There should be no damage of the outside carton box, each packaging box should have one identical label.

9.9.2. Modules inside package box should have compliant mark.

9.9.3. All direct package materials shall offer ESD protection.

Note1: Bright dot is defined as the defective area of the dot is larger than 50% of one sub-pixel area.





Bright dot: The bright dot size defect at black display pattern. It can be recognized by 2% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Dark dot: Cyan, Magenta or Yellow dot size defect at white display pattern. It can be recognized by 5% transparency of filter when the distance between eyes and panel is 350mm±50mm.

Note2: Mura on display which appears darker / brighter against background brightness on parts of display area.

10. Reliability Specification

No	Item	Condition	Quantity	Criteria
1	High Temperature Operating	70°C, 96Hrs	2	GB/T2423.2 -2008
2	Low Temperature Operating	-20°C, 96Hrs	2	GB/T2423.1 -2008
3	High Humidity Storage	50°C, 90%RH, 96Hrs	2	GB/T2423.3 -2016
4	High Temperature Storage	80°C, 96Hrs	2	GB/T2423.2 -2008
5	Low Temperature Storage	-30°C, 96Hrs	2	GB/T2423.1 -2008
6	Thermal Cycling Test Storage	-20°C, 60min ~ 70°C, 60min, 20 cycles.	2	GB/T2423.22 -2012
7	Packing vibration	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction.	-	GB/T5170.14 -2009
8	Electrical Static Discharge	Air:±4KV 150pF/330Ω 5 times Contact:±2KV 150pF/330Ω 5 times	2	GB/T17626.2 -2018
9	Drop Test (Packaged)	Height:80 cm,1 corner, 3 edges, 6 surfaces.	-	GB/T2423.8 -1995

Note1. No defection cosmetic and operational function allowable.

Note2. Total current Consumption should be below double of initial value

11. Precautions and Warranty

11.1. Safety

11.1.1. The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.1.2. Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

11.2. Handling

11.2.1. Reverse and use within ratings in order to keep performance and prevent damage.

11.2.2. Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

11.3. Storage

11.3.1. Do not store the LCD module beyond the specified temperature ranges.

11.3.2. Strong light exposure causes degradation of polarizer and color filter.

11.4. Metal Pin (Apply to Products with Metal Pins)

11.4.1. Pins of LCD and Backlight

11.4.1.1. Solder tip can touch and press on the tip of Pin LEAD during the soldering

11.4.1.2. Recommended Soldering Conditions

Solder Type: Sn96.3~94-Ag3.3~4.3-Cu0.4~1.1

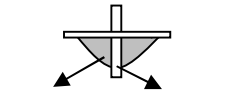
Maximum Solder Temperature: 370℃

Maximum Solder Time: 3s at the maximum temperature

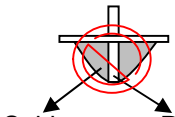
Recommended Soldering Temp: 350±20℃

Typical Soldering Time: ≤3s

11.4.1.3. Solder Wetting



Recommended



Not Recommended

11.4.2. Pins of EL

11.4.2.1. Solder tip can touch and press on the tip of EL leads during soldering.

11.4.2.2. No Solder Paste on the soldering pad on the motherboard is recommended.

11.4.2.3. Recommended Soldering Conditions

Solder type: Nippon Alimit Leadfree SR-34, size 0.5mm

Recommended Solder Temperature: 270～290℃

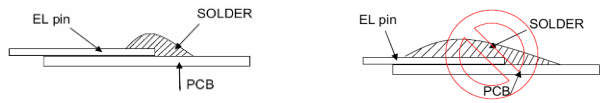
Typical Soldering Time: ≤2s

Minimum solder distance from EL lamp (body):2.0mm

11.4.2.4. No horizontal press on the EL leads during soldering.

11.4.2.5. 180° bend EL leads three times is not allowed.

11.4.2.6. Solder Wetting

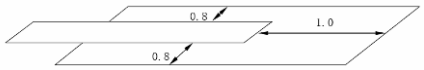


Recommended Not Recommended

11.4.2.7. The type of the solder iron:

Recommended Not Recommended

11.4.2.8. Solder Pad



11.5. Operation

11.5.1. Do not drive LCD with DC voltage

11.5.2. Response time will increase below lower temperature

11.5.3. Display may change color with different temperature

11.5.4. Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

11.5.5. Do not connect or disconnect the LCM to or from the system when power is on.

11.5.6. Never use the LCM under abnormal condition of high temperature and high humidity.

11.5.7. Module has high frequency circuits. Sufficient suppression to the electromagnetic interface shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

11.5.8. Do not display the fixed pattern for long time（we suggest the time not longer than one hour）because it will develop image sticking due to the TFT structure.

11.6. Static Electricity

11.6.1. CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

11.6.2. The normal static prevention measures should be observed for work clothes and benches.

11.6.3. The module should be kept into anti-static bags or other containers resistant to static for storage.

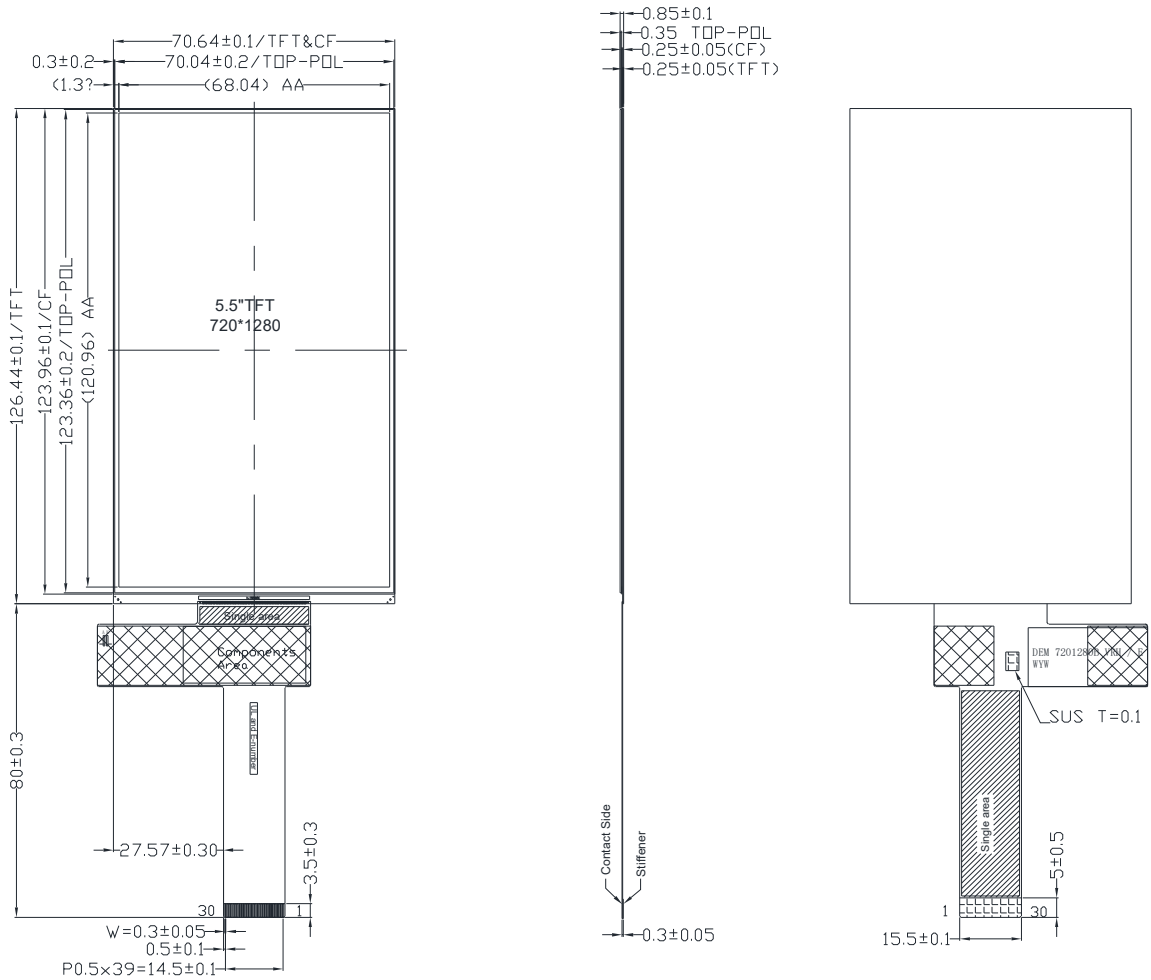
11.7. Limited Warranty

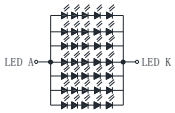
11.7.1. Our warranty liability is limited to repair and/or replacement. We will not be responsible for any consequential loss.

11.7.2. If possible, we suggest customer to use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

11.7.3. After the product shipped, any product quality issues must be feedback within three months, otherwise, we will not be responsible for the subsequent or consequential events.

12. Outline Drawing





NO.	PIN NAME
1	MTP_PWR
2	GND
3	D3N
4	D3P
5	GND
6	D2N
7	D2P
8	GND
9	D1N
10	D1P
11	GND
12	D0N
13	D0P
14	GND
15	CLKN
16	CLKP
17	GND
18	NC
19	NC
20	NC
21	IM0
22	GND
23	XRES
24	LEDPWM
25	VCI
26	IOVCC
27	NC
28	GND
29	NC(LEDA)
30	NC(LEDK)