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Revision History

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* Description

4.39" is a color active matrix AMOLED module using Low Temperature Poly-silicon Thin Film Transistors as active switching devices. The resolution of a 4.39" AMOLED contains 568xRGBx1210 Pixels and can display up to 16.7 Million colors.

1. General Specifications

	Feature	Spec	Remark
	Screen Size (Inch)	4.39	-
	FeatureSpecScreen Size (Inch)4.39Display ModeAMOLEDDisplay ModeAMOLEDResolution (Dot)568 x 1210Active Area (mm)47.3712 x 100.914Pixel Pitch (mm)0.0834 x 0.0834Pixel Pitch (mm)0.0834 x 0.0834Color Depth16.7 MillionInterfaceMIPI 2-LANEPolarizer Surface TreatmentHC CoatingharacteristicsWith TP/Without TPModule Outline Dimension(W x H x D) (mm)49.13 x 103.55 x 0.75 (mm)LectronicTouch IC(Type)SD5207Frame Rate60Hz	-	
Display	Resolution (Dot)	568 x 1210	-
Specification	Active Area (mm)	47.3712 x 100.914	-
opcomotion	Pixel Pitch (mm)	0.0834 x 0.0834	-
	Technology Type	LTPS	-
	Color Depth	16.7 Million	-
	Interface	MIPI 2-LANE	-
	Polarizer Surface Treatment	HC Coating	-
Mechanical	With TP/Without TP	With TP(on Cell)	-
Characteristics	Module Outline Dimension(W x H x D) (mm)	MIP12-LANEreatmentHC Coatingut TPWith TP(on Cell)on(W x H x D)49.13 x 103.55 x 0.75	-
	Driver IC(Type)	SD5207	-
Electronic	Touch IC(Type)	CST3530	-
	Frame Rate	60Hz	-

Note 1: Requirements on Environmental Protection: RoHS

2. Outline Dimension



3. Input/output Terminals

3.1 Main TP-FPC Pin Assignment

Number	Signal	Description	I/O
1	ELVDD		
2	ELVDD	AMOLED EL Positive power	Р
3	ELVDD		
4	ELVSS		
5	ELVSS	AMOLED EL Negative power	Р
6	ELVSS		
7	GND	Ground	Р
8	AVDD	AMOLED charge pumping power for DDIC	Р
9	NC	No Connection	
10	GND	Ground	Р
11	GND	Ground	Р
12	D0P	MIPI Data Line	I
13	NC	No Connection	
14	D0N	MIPI Data Line	I
15	GND	Ground	Р
16	GND	Ground	Р
17	GND	Ground	Р
18	CLKP	MIPI CLK Line	I
19	NC	No Connection	
20	CLKN	MIPI CLK Line	I
21	GND	Ground	Р
22	GND	Ground	Р
23	GND	Ground	Р
24	D1P	MIPI Data Line	I
25	NC	No Connection	
26	D1N	MIPI Data Line	I
27	GND	Ground	Р
28	GND	Ground	Р
29	IOVCC	AMOLED logic power for DDIC	Р
30	RESX	Drive IC reset	I
31	VCI	AMOLED logic power for DDIC	Р
32	AVDD_EN	AVDD enable	I
33	TP_VCI	Analog Power for Touch Panel	Р
34	SWIRE	Control the PMIC	

Product Specification

35	TP_RST	Reset Pin for Touch Panel	Ι
36	TE1	Tear Effect	I
37	TP_SCL	Serial Clock Signal for Touch Panel I2C I/F	I
38	TP_SDA	Serial Data Signal for Touch Panel I2C I/F	I
39	TSP_INT	Interrupt Signal for Touch Panel	I

3.2 MCU and Display Module Interface Conflagration

Power Block	VBAT VDDIO GND TSP_AVDD TSP_VDDIO	Power Block
MIPI Interface	DOP DON CLKP CLKN D1N D1P	Display
I ² C	TSP_SCL TSP_SDA TSP_INT TSP_RESET	TSP

4. AMOLED Optical Characteristics

4.1 Optical specification

ltem		Symbol	Condition	Min.	Тур.	Max.	Unit.	Note
Contrast F	Ratio	CR			100000:1			(1)(2)
Response Time	Rising Falling	T _{R+} T _F				2	msec	(1)(3)
Color Ga	mut	S(%)		97	100		%	
Brightness Ur	niformity	W255		85			%	(5)
Brightne	ess	Вр		550	600		cd/m2	
		Wx	Θ=0		0.300			
Color Filter Chromacicity	White	W _Y	Normal	-0.02	0.310	+0.02		
	Red	R _x	Angle	-0.03	0.682	+0.04		
		R _Y			0.315			(1)(4)
	Green	G _X			0.236			
		G _Y			0.722			
		Bx			0.138			
	Blue	By			0.046			
		ΘL		75	80			
Viewing	Hor.	ΘR		75	80			(1)(A)
Angle		ΘU	CR>10	75	80		Degree	(1)(4)
	Ver.	ΘD		75	80			
l	_ifetime		Ta=25°C	20000			hrs	

Measuring Condition

Measuring surrounding: dark room

Ambient temperature: 25°C±2°C

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle:



Note (2): Definition of Contrast Ratio (CR): measured at the center point of panel

CR = Luminance with all pixels white Luminance with all pixels black



Note (3): Response Time:

Note (4): Definition of optical measurement setup



Note (5): Luminance Uniformity of these 9 points is defined as below:



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Maximum Ratings (Voltage Referenced to VSS) VSS=0V, Ta=25°C

ltem	Symbol	Min.	Max.	Unit	Note
Analog Power Supply	VCI	0	+4	V	Note1
Logic Power Supply	VDDIO=IOVCC	0	+4	V	_
Analog Power Supply	AVDD	0	+10	V	-
Positive Power Input	ELVDD	-	+5.0	V	-
Negative Power Input	ELVSS	-5.0	-	V	-

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

ltem		Symbol	Min.	Тур.	Max.	Unit
Logic Power Supply		VDDIO=IOVCC	1.65	1.80	1.98	V
Analog Powe	r Supply	VCI	2.65	3.0	3.60	V
Analog Powe	r Supply	AVDD	-	7.6	-	V
Default Positive Output Voltage		ELVDD		4.60		V
Positive Output Voltage Total Variation				-		%
Default Negative Output Voltage		ELVSS		-3.50		V
Negative Output Voltage Total Variation				-		%
Input Signal Valtaga	High Level	VIH	0.70*Vddio	-	VDDIO	V
input Signal Voltage	Low Level	VIL	GND	-	Max. 1.98 3.60 - VDDIO 0.30*VDDIO VDDIO 0.20*VDDIO	V
Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V
	Low Level	VOL	GND	-	0.20*VDDIO	V

Note: The current and power consumption were tested under White pattern, 25°C

6. AC Characteristics

6.1 MIPI DC Characteristics



Figure 8-4-1-1 MIPI DC Characteristics

DC characteristics for MIPI LP mode:

Parameter	Description	Min	Nom	Max	Unit
VIH	Logic 1 input voltage	<mark>88</mark> 0			mV
VIL	Logic 0 input voltage			550	mV
VOH	Logic 1 output voltage	1	1.1	1.15	V
VOL	Logic 0 output voltage	-50	1	50	mV

DC characteristics for MIPI HS mode:

Parameter	Description	Min	Nom	Max	Unit
VCMRX(DC)	Common-mode voltage HS receive mode	70		330	mV
VIDTH	Differential input high threshold			70	mV
VIDTL	Differential input low threshold	-70			mV
VIHHS	Single-ended input high voltage	6		460	mV
VILHS	Single-ended input low voltage	-40			
ZID	Differential input impedance	80	100	120	Ω

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6.2 MIPI AC Characteristics













Turnaround Procedure



Figure 8-4-2-3 Turnaround Procedure

Product Specification

Parameter	Description	Min	тур	Max	Unit	Notes
Telk-miss	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TTRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI	č.		ns	5
Tolk-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			U	5
T _{CLK-PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
Tolk-settle	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of T _{CLK-PREPARE} .	95		300	ns	6, 7
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX} .	Time for Dn to reach VTERN-EN		38	ns	6
Telk-trail	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
T _{CLK-PREPARE} + T _{CLK-ZERO}	$T_{\text{CLK-PREPARE}}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
T _{D-TERM-EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX} .	Time for Dn to reach V _{TERM-EN}		35 ns + 4*UI		6
Теот	Transmitted time interval from the start of $T_{\text{HS-TRAIL}}$ or $T_{\text{CLK-TRAIL}}$, to the start of the LP-11 state following a HS burst.			105 ns + n*12*UI		3, 5
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5
			2			

Parameter	Description	Min	Тур	Max	Unit	Notes
Ths-prepare	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	5
THS-PREPARE + THS-ZERO	T _{HS-PREPARE} + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns	5
Тир-реттие	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS.85 ns + 6*UI145 ns + 10*UIPREPARE.The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.85 ns + 6*UI145 ns + 10*UI		ns	6		
Ths-skip	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns	6
T _{HS-TRAIL}	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3, 5
TINIT	See Section 6.11.	100			μs	5
TLPX	Transmitted length of any Low-Power state period	50			ns	4, 5
Ratio TLPX	Ratio of $T_{\text{LPX}(\text{MASTER})}/T_{\text{LPX}(\text{SLAVE})}$ between Master and Slave side	2/3		3/2		
T _{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX			ns	5
T _{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*T _{LPX}		ns	5	
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.		ns	5		
TWAKEUP	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5

6.3 Display RESET Timing

Reset Input Timing:



Figure 8-6-1 Reset Function

Symbol	Parameter	Related Pins	Min.	Тур.	Max.	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-		us
tREST	*2) Reset complete time				5	When reset applied during sleep in mode	ms
					120	When reset applied during Sleep out mode	ms

7. Recommended Operating Sequence

- 7.1 Display Power On / Off Sequence
 - 7.1.1 Power On Sequence



Figure 8-3-1-1 Power on sequence

- Note: 1.Ton: The time between the VDDIO and the VCI power on, Ton \geq 0 ms
 - 2.Dotted line is optional.
 - 3. All the power supplies should be stable during display on status.
 - 4. Current of VDDIO, VCI, AVDD should be less than 150mA respectively.



7.1.2 Power Off Sequence

7.2 Brightness Control

		Addı	ress		Description	
Inst/Para	R/W	MIPI	Other	Date Type		
BRTCTRL	W	51h	5100h	Hex	Value form 0~255(FF)	

8. Touch Specification

8.1 Touch Design

Item		Description	Notes
	Sensor Structure	Oncell (Pls contact us if you need any cover	-
		glass to realize a touch	
	Sensor Pitch	Sensor Pitch Tx:4.742mm · Rx:5.048mm	
Touch Design	Sensor Pattern	Diamond	-
	CH Number	10(Tx) / 20(Rx)	-
	CTP IC	CST3530	-

8.2 Electrical Characteristics

8.2.1 Maximum Ratings

Item	Symbol	MIN	MAX	Unit
TP Power Supply Input	TP_VCI	2.7	3.6	V

8.2.2 Power supply DC characteristics

Item	Symbol	MIN	TYP	MAX	Unit
TP Power Supply Input	TP_VCI	2.8	2.8/3.0/3.3	3.6	V

8.3 TP FPC Pin Assignment

No	Symbol	I/O	Description
1	GND	GND	Ground
2	TP_VCI	Power	Analog Power for Touch Panel
3	TP_RESET	I	Reset Pin for Touch Panel
4	TP_SDA	I/O	SDA pin for Touch Panel
5	TP_SCL	I	SCL pin for Touch Panel
6	TP_INT	0	Interrupt signal for Touch Panel

9. AMOLED Module Out-Going Quality Level

9.1 VISUAL & FUNCTION INSPECTION STANDARD

9.1.1 Inspection Conditions



9.1.2 Definition



Zone A: Effective Viewing Area (Character or Digit can be seen)

Zone B: Viewing Area except Zone A

Zone C: Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D: IC Bonding Area

Note: As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

9.1.3 Sampling Plan

According to GB/T 2828-2003; Normal Inspection, Class II AQL:

Major Defect	Minor Defect		
0.65	1.5		

No	Items to be inspected	Criteria	Classification of Defects
	Functional	 No display, Open or miss line Display abnormally, Short 	
1	defects	defects 3) Backlight no lighting, abnormal lighting. etc	
2	Missing	Missing components and etc	Major
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc	
4	Color tone	Color unevenness, refer to limited sample	
5	Spot/Line defect	Light dot,Dim spot,(Note1) Polarizer Air Bubble, Polarizer accidented spot and etc	Mipor
6	Soldering	Good soldering , Peeling off is not allowed and	WIND
	appearance	etc	
7	AMOLED	Black/White spot/line, scratch, crack, etc.	
	/Polarizer		

Note1: a) Light dot: Dots appear bright and unchanged in size in which AMOLED panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which AMOLED panel is displaying under pure red, green, blue picture.

9.1.4 Criteria (Visual)

Number	Items	Criteria(mm)				
1.0 AMOLEDCrack/BrokenNOTE:X: LengthY: WidthZ: Height	(1) The edge of AMOLE D broken					
L: Length of ITO,		X Y Z				
T: Height of AMO ELD		≤3.0mm <inner border="" line="" of<br="">the seal ≤T</inner>				
	(2)AMOLED corner broken	XYZ ≤ 3.0 mm $\leq L$ $\leq T$				
(3) AMOLED crack		Crack Not allowed				

Product Specification



3.0	AMOLED Pixel defe	rixel defe Pixel bad points					
	ct	Item	Zone A	Acceptable Qtv			
			Random	N≤2			
		Bright dot	2 dots adjacent	N≤0			
		5	3 dots adjacent	N≤0			
			Random	N≤3			
		Dark dot	2 dots adjacent	N≤0			
			3 dots adjacent	N≤0			
		Distance	 Minimum Distance Between Bright dots. Minimum Distance Between dark dots Minimum Distance Between dark and bright dot. 	5mm			
		Total bright a	N≤4				
		Note:					
		A) Bright dot	A) Bright dot: Dots appear bright and unchanged in size in whi				
		AMOLED	AMOLED panel is displaying under black pattern.				
		B) Dark dot: AMOLED picture.	Dots appear dark and unchanged in panel is displaying under pure red, g	size in which Jreen, blue			
		C) 2 dot adja Picture:	cent = 1 pair = 2 dots				
		2 dot adja	cent 2 dot adjacent				
		2 dot adjacen	t (vertical) 2 dot adjacent (s	slant)			

	Line defect (AMOLED					
	/Polarizer backlight) A / i alt la (vas vas)	Length(m	Acce	Acceptable Qty	
	black/white line,	vviatn(mm)	m)	А	В	С
	scratch, stain)	Ф≤0.05	Ignore	Ignore		
4.0		0.05 <w≤0.06< td=""><td>L≤5.0</td><td>N≤3</td><td></td><td>Ignore</td></w≤0.06<>	L≤5.0	N≤3		Ignore
	W: width, L∶length	0.07 <w≤0.08< td=""><td>L≤4.0</td><td>N≤2</td><td></td><td></td></w≤0.08<>	L≤4.0	N≤2		
	N : Count	W>0.08 Define as spot defect				
	Electronic Componen	nic Componen Not allow missing parts, solderless connection, cold solder joint, mi smatch, The positive and negative polarity opposite				
5.0	ts SMT.					
Display color& Brigh 1. Color: Measuring the color coordinates, The measurement of 0					ement standa	
	tness.	2. Brightness: Measuring the brightness of White screen, The meas urement standard according to the datasheet or Samples.				

Criteria (functional items)

Items	Criteria (mm)
No display	Not allowed
Missing segment	Not allowed
Short	Not allowed
Backlight no lighting	Not allowed
	Items No display Missing segment Short Backlight no lighting

10. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70°C, 96h	
Low Temperature Operating	-20°C, 96h	
High Temperature Storage	80°C, 96h	
Low Temperature Storage	-30°C, 96h	Inspection after 2~4hours
High Temperature &	+60°C, 90% RH ,96h	storage at room temperature, the sample shall be free from defects: 1. Air bubble in the AMOLED;
High Humidity Operating		
Thermal Shock (Non-operation)	-10°C, 30 min \leftrightarrow 60°C, 30 min, Change time: 5min 20CYC.	
C=150pF, R=330,5points/panel 3. Missi	 Non-display; Missing segments/line; 	
ESD Test	Air:±8kV, 5times; Contact:±4kV, 5 times;	4. Glass crack;
(Environment: 15°C~35°C, 30%~60%).	5. Current IDD is twice higher	
Vibration (Non-operation)	Frequency Range: 10~55Hz, Stroke:1.5mm	than initial value.
	Sweep:10Hz~55Hz~10Hz 2 hours for each	
	direction of X.Y.Z. (6 hours for total)	
	(Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM	

Remark:

- 1. The test samples should be applied to only one test item.
- 2. Sample size for each test item is 3~10pcs.
- 3. For Damp Proof Test, Pure water (Resistance > $10M\Omega$) should be used.
- 4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
- 6. The color fading mura of polarizing filter should not care.

Version: 1

11. Cautions and Handling Precautions

11.1 Handling and Operating the Module

When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

Protect the module from static; it may cause damage to the CMOS ICs.

Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

Do not disassemble the module.

Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

Pins of I/F connector shall not be touched directly with bare hands.

Do not connect, disconnect the module in the "Power ON" condition.

11.2 Storage and Transportation.

Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0°C to 35°C

and relative humidity of less than 70%

Do not store the AMOLED module in direct sunlight.

The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

It is recommended that the modules should be stored under a condition where no condensation is allowed.

Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.