

Display Elektronik GmbH

# DATA SHEET

OLED MODULE

**DEP 7201280A-RGB**

4,97" AM-OLED

Product Specification

Version: 1

10.05.2025



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## 1 Features

### 1.1 Product Applications

mobile phone, portable GPS, handheld game console ...

### 1.2 Product Features

**1.2.1** Display Color: 16.7 Million (RGB x 8 Bits)

**1.2.2** Display Format: 4.97"HD (720 x RGB x 1280)

**1.2.3** Pixel Arrangement: Rendering

**1.2.4** Interface: MIPI 4 Lanes

**1.2.5** Driver IC: RM67295 (Raydium)

**1.2.6** Touch IC: CHSC5448

**1.2.7** Touch screen: On-Cell (Pls contact us in case of any custom touch glass required)

**1.2.8** Polarizer: Hard Coating Polarizer

## 2 Mechanical Specifications

| Item                                            | Specification                | Unit |
|-------------------------------------------------|------------------------------|------|
| Dimension Outline                               | 64.12 x 116.72 x 0.94        | mm   |
| Encapsulation Outline                           | 64.12 x 113.82               | mm   |
| Resolution                                      | 720 x RGB x 1280 (Rendering) | Dots |
| Active Area                                     | 61.884 x 110.016             | mm   |
| Diagonal Size                                   | 4.97                         | Inch |
| Pixel Pitch                                     | 28.65 x 85.95                | μm   |
| Glass Thickness<br>(LTPS / Encapsulation Glass) | 0.20 / 0.30                  | mm   |
| Weight                                          | ~ 14                         | g    |

### 3 Maximum Rating

| Parameter                   | Symbol | Spec |      |      | Unit | Note |
|-----------------------------|--------|------|------|------|------|------|
|                             |        | Min. | Typ. | Max. |      |      |
| Analog/ boost Power Voltage | VCI    | -0.3 | -    | 5.5  | V    | -    |
| I/O Voltage                 | VDDIO  | -0.3 | -    | 5.5  | V    | -    |
| Power IC Input Voltage      | VBAT   | -0.3 | -    | 6    | V    | -    |
| Operating Temperature       | Top    | -20  | -    | 70   | °C   | -    |
| Storage Temperature         | Tstg   | -30  | -    | 80   | °C   | -    |
| Power Consumption           | -      | -    | 2000 | 2300 | mW   | -    |

### 4 Electrical Specifications

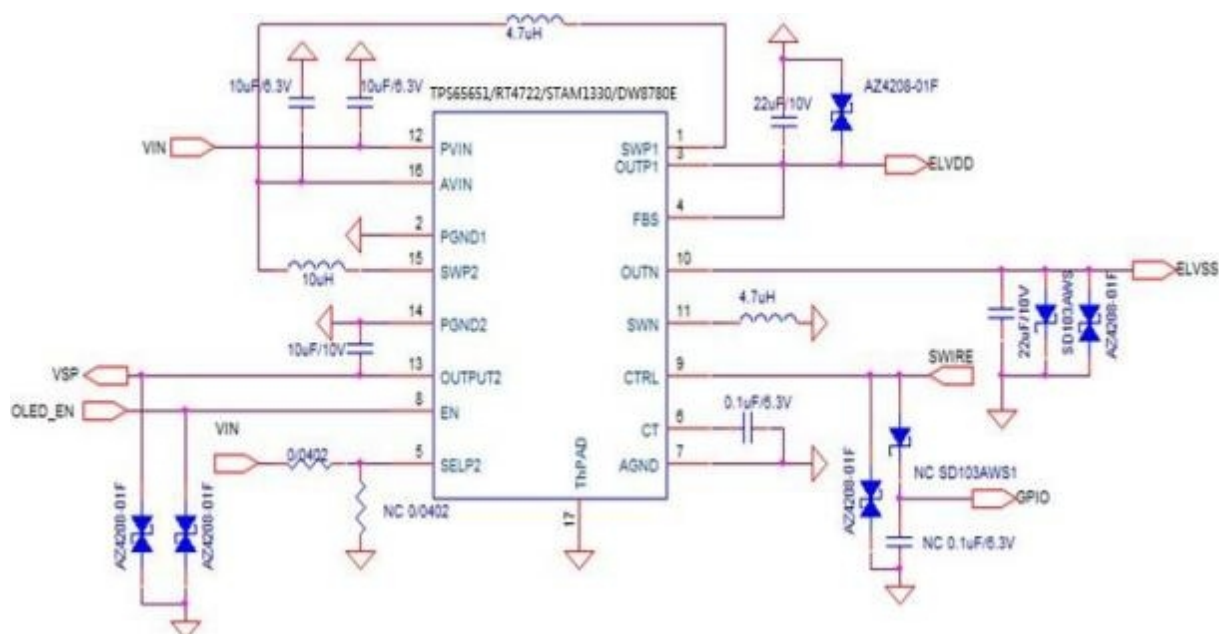
#### 4.1 Electrical Characteristics

##### 4.1.1 Current Characteristic

| Item                    | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-------------------------|--------|------|------|------|------|--------|
| Power IC Input Voltage  | VBAT   | 2.9  | -    | 4.5  | V    | Ref    |
| Digital Power Supply    | VDDI   | 1.65 | 1.8  | 3.6  | V    | Ref    |
| Analog Power Supply     | VCI    | 2.5  | 3.3  | 4.8  | V    | Ref    |
| TP Power Supply Voltage | AVDD   | 2.7  | -    | 3.6  | V    | -      |
| TP I/O Digital Voltage  | Iovcc  | 1.65 | -    | 3.6  | V    | -      |

| Mode                    | Symbol | Condition                                                      | Min. | Typ. | Max. | Unit | Remark |
|-------------------------|--------|----------------------------------------------------------------|------|------|------|------|--------|
| Full White<br>@350 Nits | IVBAT  | IVBAT=4V<br>VCI=3.3V<br>VDDIO=1.8V<br>@ Full white<br>450 nits | -    | 300  | 380  | mA   | -      |
|                         | IVCI   |                                                                | -    | 2    | 3    | mA   | -      |
|                         | IVDDIO |                                                                | -    | 15   | 20   | mA   | -      |
| TP Normal<br>Operation  | Iopr   | AVDD=3.3V<br>Iovcc = 1.8V                                      |      | 16   |      | mA   | -      |
| TP Monitor              | Imon   |                                                                |      | 0.6  |      | mA   | -      |
| TP Sleep                | Islp   |                                                                |      | 40   |      | uA   | -      |

## 4.1.3 Application Circuit



## 4.2 I/O Connection and Block Diagrams

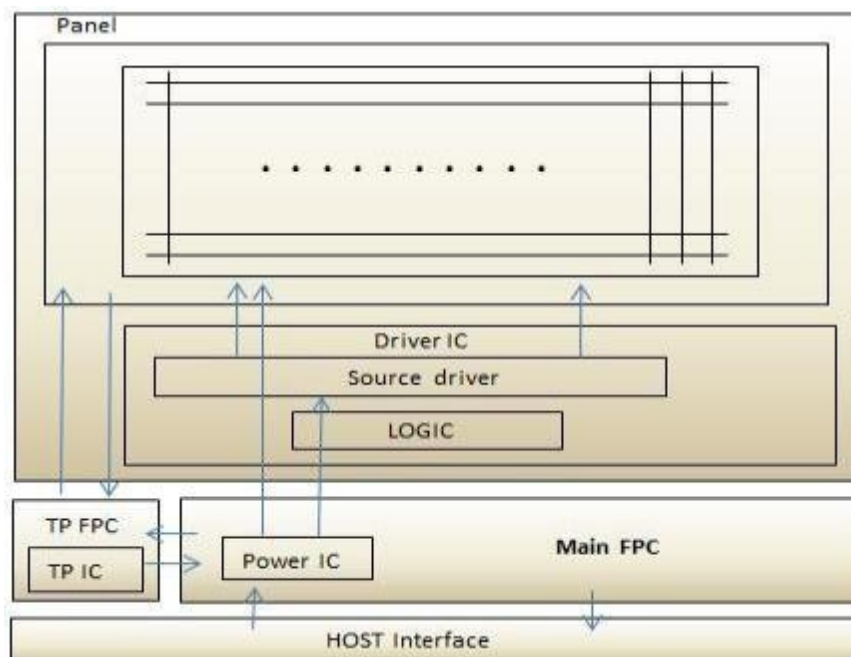
## 4.2.1 I/O Connection

| #  | Pin Name | I/O   | Description                                                                                        |
|----|----------|-------|----------------------------------------------------------------------------------------------------|
| 1  | GND      | Power | The power ground                                                                                   |
| 2  | VBAT     | Power | Power IC Input Voltage                                                                             |
| 3  | VBAT     | Power | Power IC Input Voltage                                                                             |
| 4  | VBAT     | Power | Power IC Input Voltage                                                                             |
| 5  | VBAT     | Power | Power IC Input Voltage                                                                             |
| 6  | VBAT     | Power | Power IC Input Voltage                                                                             |
| 7  | GND      | Power | The power ground                                                                                   |
| 8  | GND      | Power | The power ground                                                                                   |
| 9  | GND      | Power | The power ground                                                                                   |
| 10 | MTP_PWR  | Power | Power supply for OTP.<br>Leave the pin to open when not in use.                                    |
| 11 | TE       | O     | Tear effect output                                                                                 |
| 12 | RESX     | I     | This signal will reset the device and must be applied to properly initialize the chip. Active low. |
| 13 | VDDIO    | Power | Driver IC digital I/O supply                                                                       |

|    |         |       |                                                                |
|----|---------|-------|----------------------------------------------------------------|
| 14 | GND     | Power | The power ground                                               |
| 15 | D2P     | I/O   | MIPI DSI data2+                                                |
| 16 | D2N     | I/O   | MIPI DSI data2-                                                |
| 17 | GND     | Power | The power ground                                               |
| 18 | D1P     | I/O   | MIPI DSI data1+                                                |
| 19 | D1N     | I/O   | MIPI DSI data1-                                                |
| 20 | GND     | Power | The power ground                                               |
| 21 | CLKP    | I     | MIPI DSI clock+                                                |
| 22 | CLKN    | I     | MIPI DSI clock-                                                |
| 23 | GND     | Power | The power ground                                               |
| 24 | D0P     | I/O   | MIPI DSI data0+                                                |
| 25 | D0N     | I/O   | MIPI DSI data0-                                                |
| 26 | GND     | Power | The power ground                                               |
| 27 | D3P     | I/O   | MIPI DSI data3+                                                |
| 28 | D3N     | I/O   | MIPI DSI data3-                                                |
| 29 | GND     | Power | The power ground                                               |
| 30 | VCI     | Power | Driver IC analog supply                                        |
| 31 | GND     | Power | The power ground                                               |
| 32 | TP_VCC  | Power | TP IC digital power supply                                     |
| 33 | TP_VDDI | Power | TP IC digital I/O supply                                       |
| 34 | TP_INT  | I/O   | Interrupt request to the host, orWakeup request from the host. |
| 35 | TP_SDA  | I/O   | I2C Data Input & Output                                        |
| 36 | TP_SCL  | I/O   | I2C Clock Input                                                |
| 37 | TP_RESX | I     | External Reset,Low is Active                                   |
| 38 | NC      | /     | NC                                                             |
| 39 | GND     | Power | The power ground                                               |
|    |         |       |                                                                |



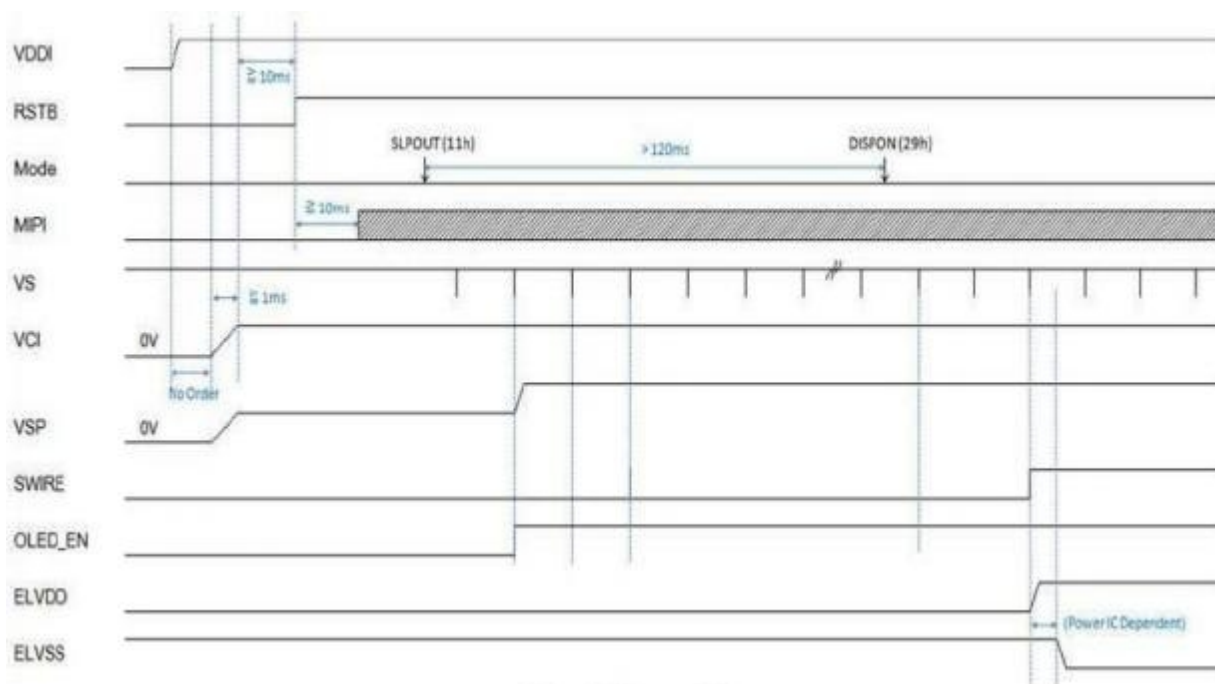
#### 4.2.2 Display Module Block Diagram



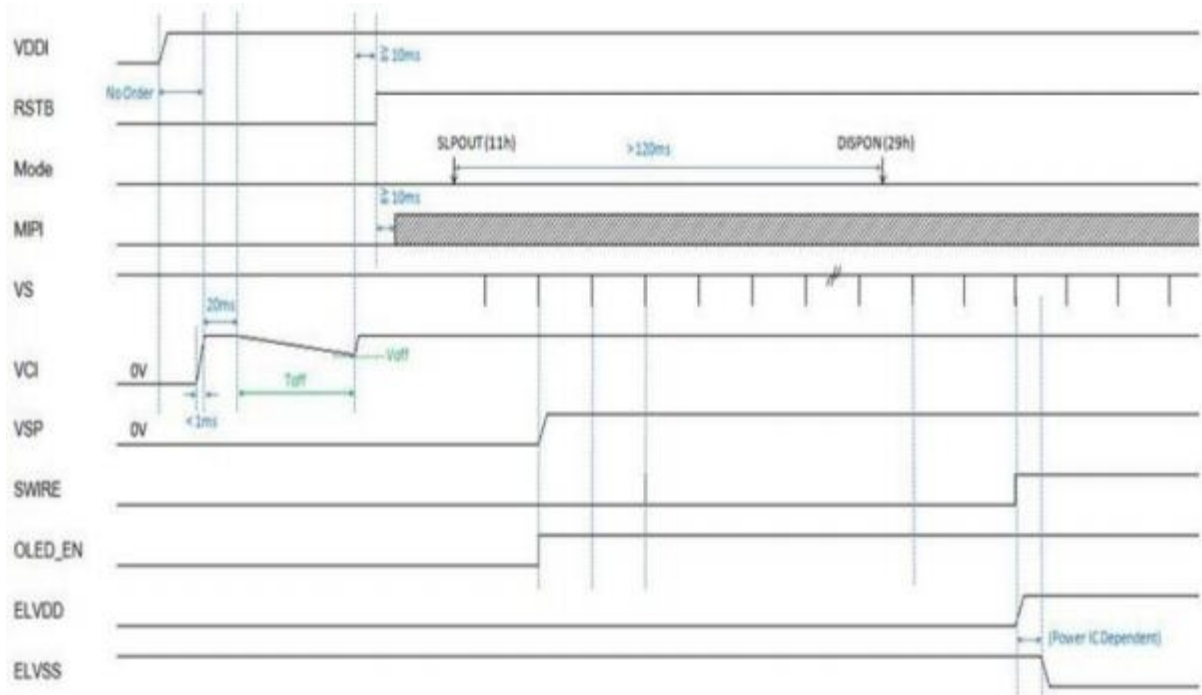
### 4.3 Recommended Operating Sequence

#### 4.3.1 Power On Sequence

Power ON for Normal VCI Case:  $T_r > 1\text{ms}$



Power ON for fast VCI Case:  $T_r < 1\text{ms}$



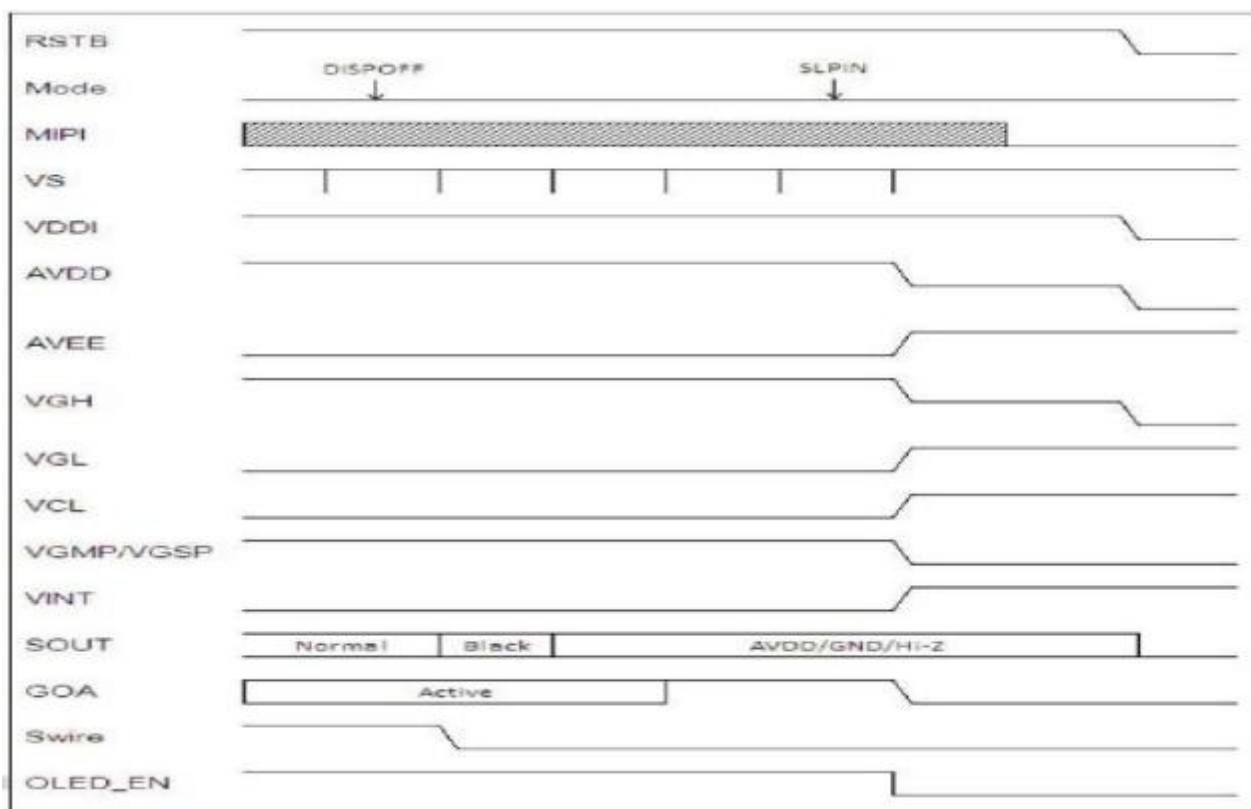
Note: If VCI's rising time is smaller than 1ms, it is suggested to use VCI H-L-H sequence to avoid the start-up issue due to fast VCI ramp up.

-- the 1<sup>st</sup> H is suggested to be 20ms

-- the L period is the time that can make Voff in between 2.6V and 1.5V.

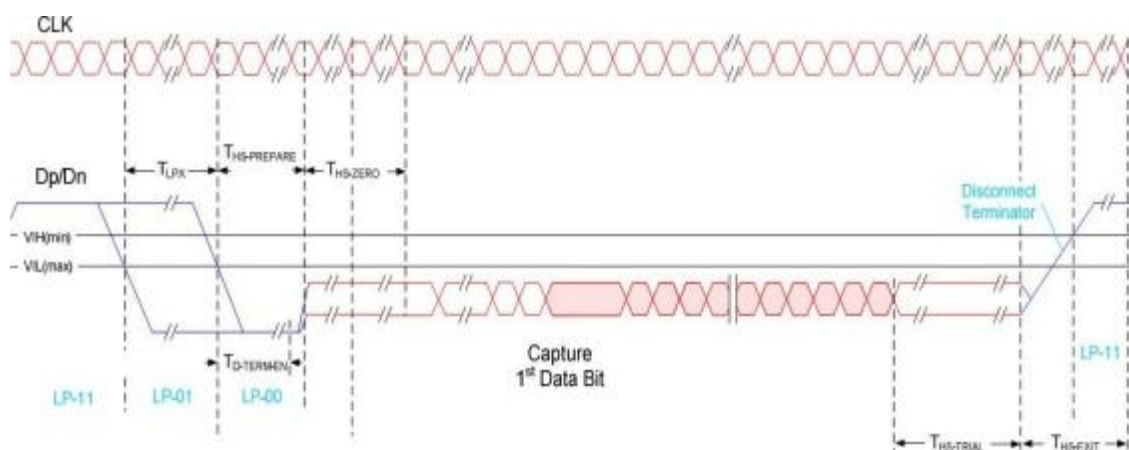
(for example, when the discharge time is 20ms and 200ms for VCI to drop below 2.6V and 1.5V, respectively. Then the Toff is suggested to be  $>20\text{ms}$  and  $<200\text{ms}$ .)

### 4.3.2 Power Off Sequence

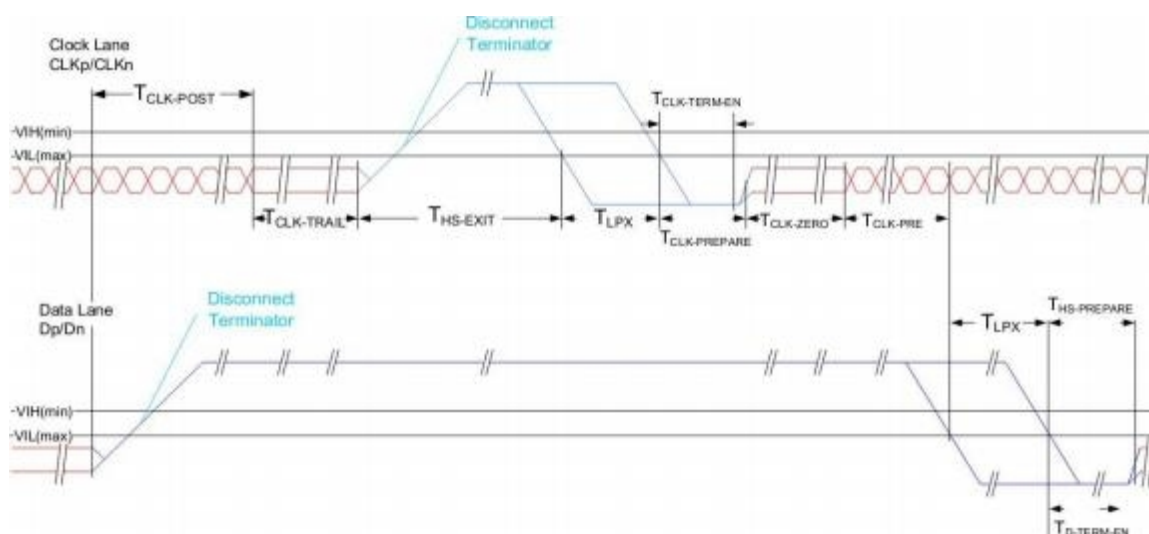


## 4.4 AC Characteristics ( MIPI )

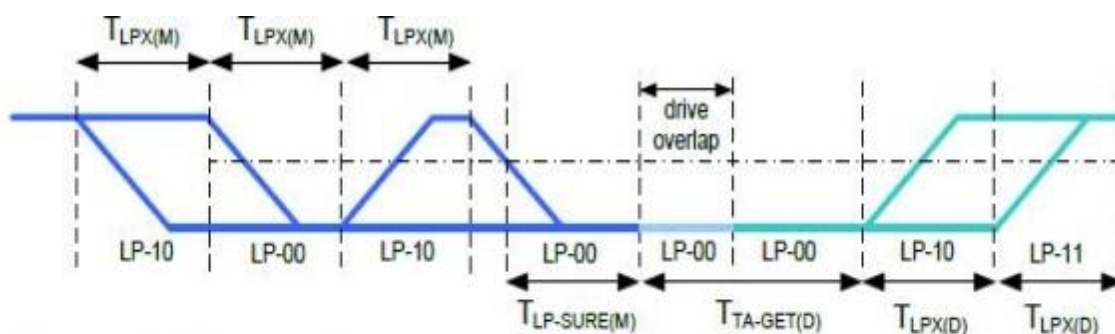
### 4.4.1 HS Data Transmission Burst



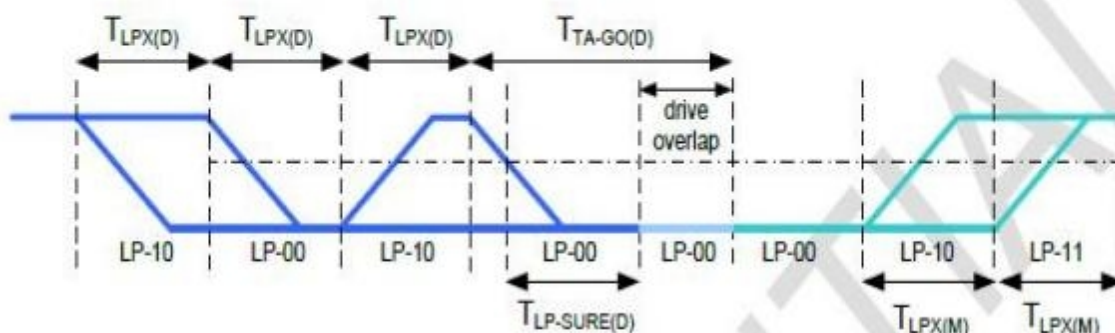
## 4.4.2 HS Clock Transmission



## 4.4.3 Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

## 4.4.4 Timing Parameters

## Timing Parameters:

| Parameter                        | Description                                                                                                                                                                                                                  | Min                                | Typ | Max            | Unit |
|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|-----|----------------|------|
| $T_{CLK-POST}$                   | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$ . | $60ns + 52*UI$                     |     |                | ns   |
| $T_{CLK-TRAIL}$                  | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.                                                                                                                 | 60                                 |     |                | ns   |
| $T_{HS-EXIT}$                    | Time that the transmitter drives LP-11 following a HS burst.                                                                                                                                                                 | 300                                |     |                | ns   |
| $T_{CLK-TERM-EN}$                | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ .                                                                                              | Time for Dn to reach $V_{TERM-EN}$ |     | 38             | ns   |
| $T_{CLK-PREPARE}$                | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.                                                                                        | 38                                 |     | 95             | ns   |
| $T_{CLK-PRE}$                    | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.                                                                                     | 8                                  |     |                | UI   |
| $T_{CLK-PREPARE} + T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.                                                                                                                             | 300                                |     |                | ns   |
| $T_{D-TERM-EN}$                  | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ .                                                                                               | Time for Dn to reach $V_{TERM-EN}$ |     | $35 ns + 4*UI$ |      |
| $T_{HS-PREPARE}$                 | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission                                                                                          | $40ns + 4*UI$                      |     | $85 ns + 6*UI$ | ns   |
| $T_{HS-PREPARE} + T_{HS-ZERO}$   | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.                                                                                                                  | $145ns + 10*UI$                    |     |                | ns   |
| $T_{HS-TRAIL}$                   | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst                                                                                                       | $60ns + 4*UI$                      |     |                | ns   |



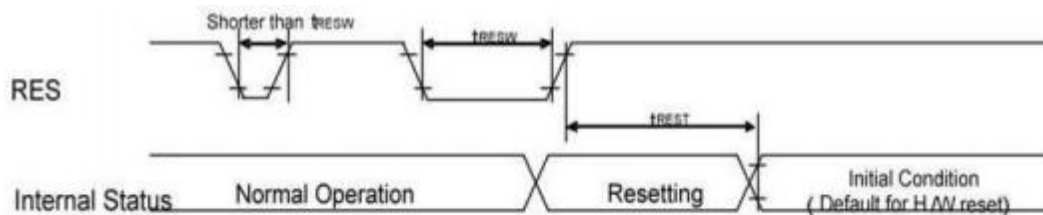
## Low Power Mode :

| Parameter        | Description                                                                                                                     | Min          | Typ                  | Max                  | Unit | Notes |
|------------------|---------------------------------------------------------------------------------------------------------------------------------|--------------|----------------------|----------------------|------|-------|
| $T_{LPX(M)}$     | Transmitted length of any Low-Power state period of MCU to display module                                                       | 50           |                      | 150                  | ns   | 1,2   |
| $T_{TA-SURE(M)}$ | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(M)}$ |                      | $2 \cdot T_{LPX(M)}$ | ns   | 2     |
| $T_{LPX(D)}$     | Transmitted length of any Low-Power state period of display module to MCU                                                       | 50           |                      | 150                  | ns   | 1,2   |
| $T_{TA-GET(D)}$  | Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.                  |              | $5 \cdot T_{LPX(D)}$ |                      | ns   | 2     |
| $T_{TA-GO(D)}$   | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.                 |              | $4 \cdot T_{LPX(D)}$ |                      | ns   | 2     |
| $T_{TA-SURE(D)}$ | Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.            | $T_{LPX(D)}$ |                      | $2 \cdot T_{LPX(D)}$ | ns   | 2     |

## NOTE:

1.  $T_{LPX}$  is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

## 4.4.5 Timing Requirements for RESETB



## Reset input timing:

IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C

| Symbol     | Parameter                 | Related Pins | MIN | TYP | MAX | Note                                     | Unit    |
|------------|---------------------------|--------------|-----|-----|-----|------------------------------------------|---------|
| $t_{RESW}$ | *1) Reset low pulse width | RESX         | 10  | -   | -   | -                                        | $\mu s$ |
| $t_{REST}$ | *2) Reset complete time   | -            | -   | -   | 5   | When reset applied during Sleep in mode  | ms      |
|            |                           | -            | -   | -   | 120 | When reset applied during Sleep out mode | ms      |

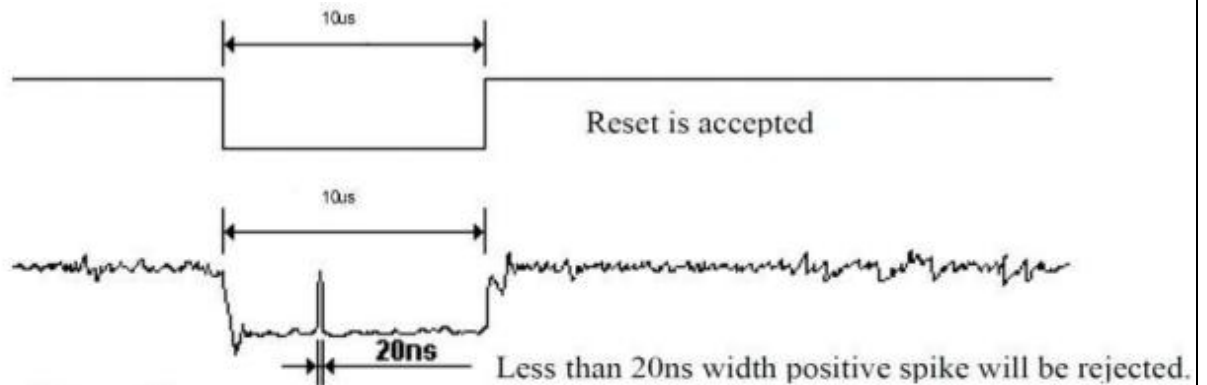
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

| RESX Pulse                       | Action                                                             |
|----------------------------------|--------------------------------------------------------------------|
| Shorter than 5 $\mu s$           | Reset Rejected                                                     |
| Longer than 10 $\mu s$           | Reset                                                              |
| Between 5 $\mu s$ and 10 $\mu s$ | Reset starts<br>(It depends on voltage and temperature condition.) |

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time ( $t_{REST}$ ) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

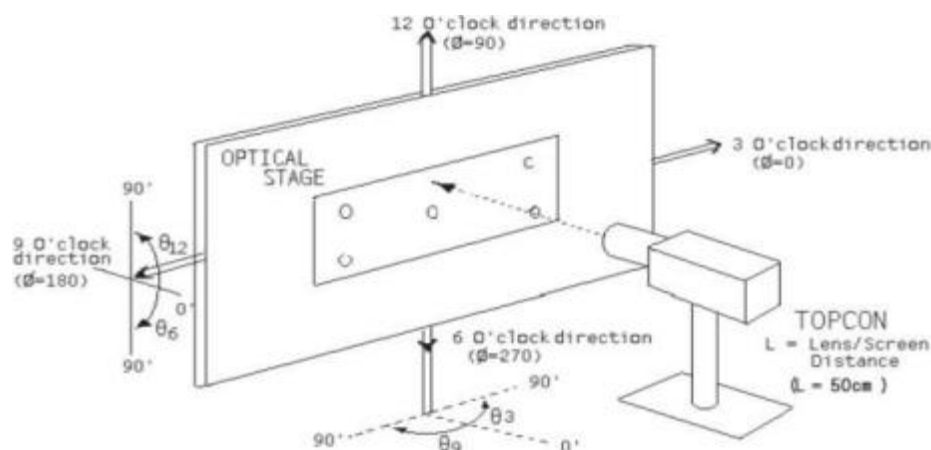
## 5 Electro-Optical Specification

| Item                  | Symbol |    | Conditions                                     | Min.     | Typ. | Max.  | Unit  | Remark  |
|-----------------------|--------|----|------------------------------------------------|----------|------|-------|-------|---------|
| Brightness            |        |    | L255                                           | 450      | 500  | .     | cd/m² | Note1   |
| Brightness Uniformity |        |    | L255                                           | 75       |      | .     | %     | Note2   |
| Contrast Ratio        |        | CR | Normal to surface                              | 60.000:1 |      | .     | .     | Note3   |
| CIE Chromaticity      | White  | x  | Normal to surface                              | 0.27     | 0.29 | 0.31  | .     |         |
|                       |        | y  |                                                | 0.29     | 0.31 | 0.33  | .     |         |
|                       | Red    | x  |                                                | 0.64     | 0.67 | 0.70  | .     |         |
|                       |        | y  |                                                | 0.30     | 0.33 | 0.36  | .     |         |
|                       | Green  | x  |                                                | 0.15     | 0.20 | 0.25  | .     |         |
|                       |        | y  |                                                | 0.67     | 0.72 | 0.77  | .     |         |
|                       | Blue   | x  |                                                | 0.09     | 0.13 | 0.17  | .     |         |
|                       |        | y  |                                                | 0.02     | 0.06 | 0.10  | .     |         |
| Color Gamut           |        |    | vs. NTSC                                       | 90       | 105  |       | %     |         |
| Viewing angle         |        |    | U/D/L/R CR≥ 1000                               | 80       |      | .     | °     |         |
| Color shift (JNCD)    |        |    | @ 45 degree                                    |          |      | 6     |       | Note4   |
| Cross-talk            |        |    |                                                |          |      | 2     | %     | Note5   |
| Gamma                 |        |    | V(Gray)=<br>48,72,104, 132,164,<br>192,224,255 | 2.0      | 2.2  | 2.4   | .     |         |
| Response time         |        |    |                                                | .        | .    | 2     | ms    | Note6   |
| Color Temperature     |        |    |                                                | 6537     | 7437 | 8337  | K     |         |
| Flicker               |        |    | Normal<br>Θ = Φ = 0 °                          |          |      | -40   | dB    | Note 7  |
| Image Retention       |        |    |                                                |          |      | 3     | min   | Note 8  |
| Image Sticking        |        |    |                                                |          |      | 3     | hrs   | Note 9  |
| Color Uniformity      |        |    | Full White Δ u'v'                              |          |      | 0.012 |       | Note 10 |
| Lifetime              |        |    | Ta=25°C                                        | 20000    |      |       | Hrs   |         |



**Note1: Temp.25°C, (Angle 、 distance)**

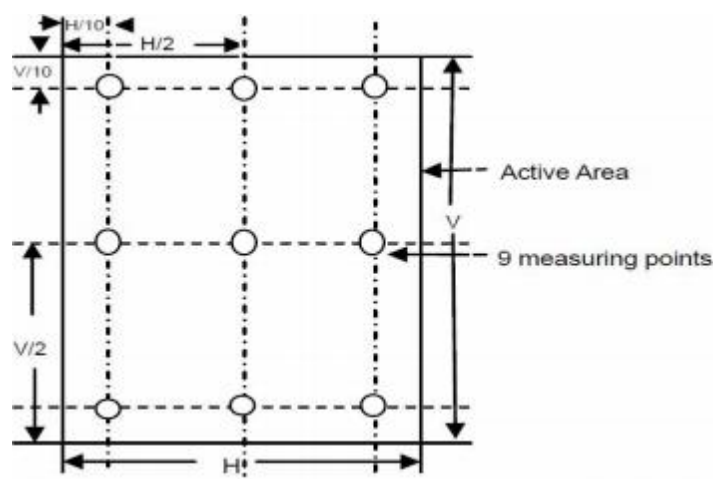
Environmental conditions: Temp.25°C±3°C, 65%±20%RH, Dark Room.  
Distance of OLED display center to measuring machine is 50cm.



**Note2: Brightness Uniformity definition**

Measure 9 points of Display Brightness,

$$\text{Luminance uniformity} = \frac{(\text{Min Luminance of 9 points})}{(\text{Max Luminance of 9 points})} \times 100\%$$



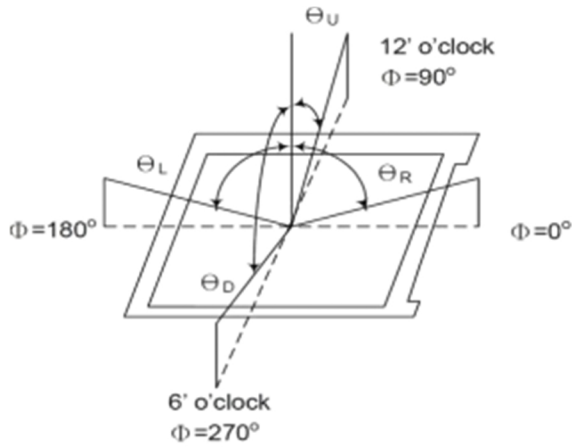
**Note3: Contrast Ratio**

Dark Room C.R=LW/LB

LW: full white brightness of display center P0;

LB : full black brightness of display center P0.

Contrast Ratio Uniformity = CRmin / CRmax



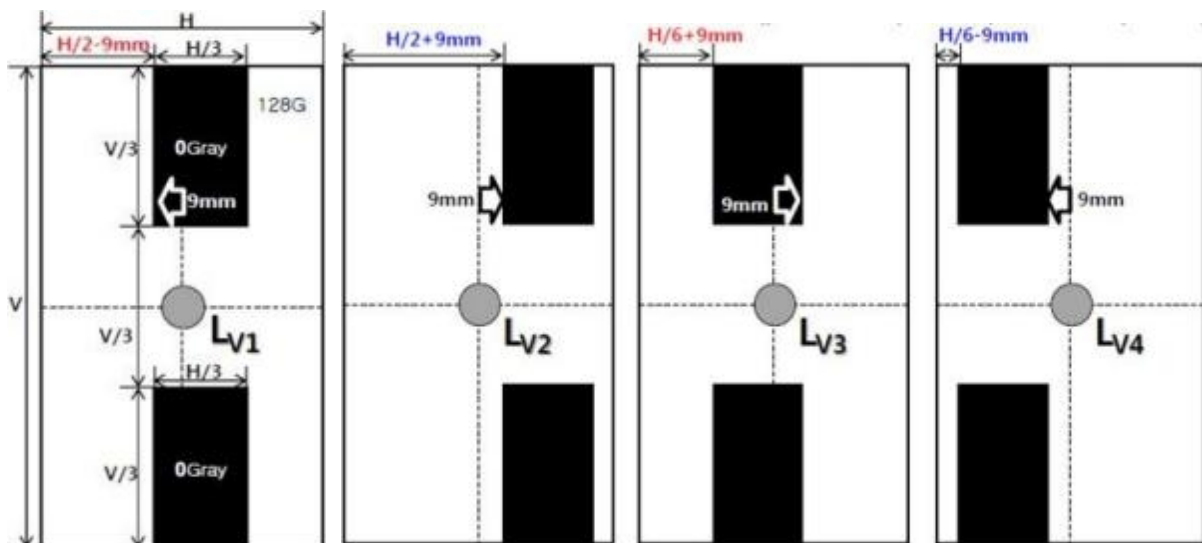
**Note4: Color Shift JNCD**

- For JNCD measure:
- Fix on the white pattern,
- On the condition  $\theta=0$   $F=0^\circ$ , we can get the color coordinate  $(u_1', v_1')$  and on  $\theta F=45^\circ$  we can get another color coordinate  $(u_2', v_2')$
- $\Delta = \text{Square Root}((u_2' - u_1')^2 + (v_2' - v_1')^2)$
- JNCD stands for "Just Noticeable Color Difference"
- For the  $(u', v')$  color space  $\text{JNCD}=0.0040$ .
- 4 JNCD means  $\Delta u'v' < 0.016$

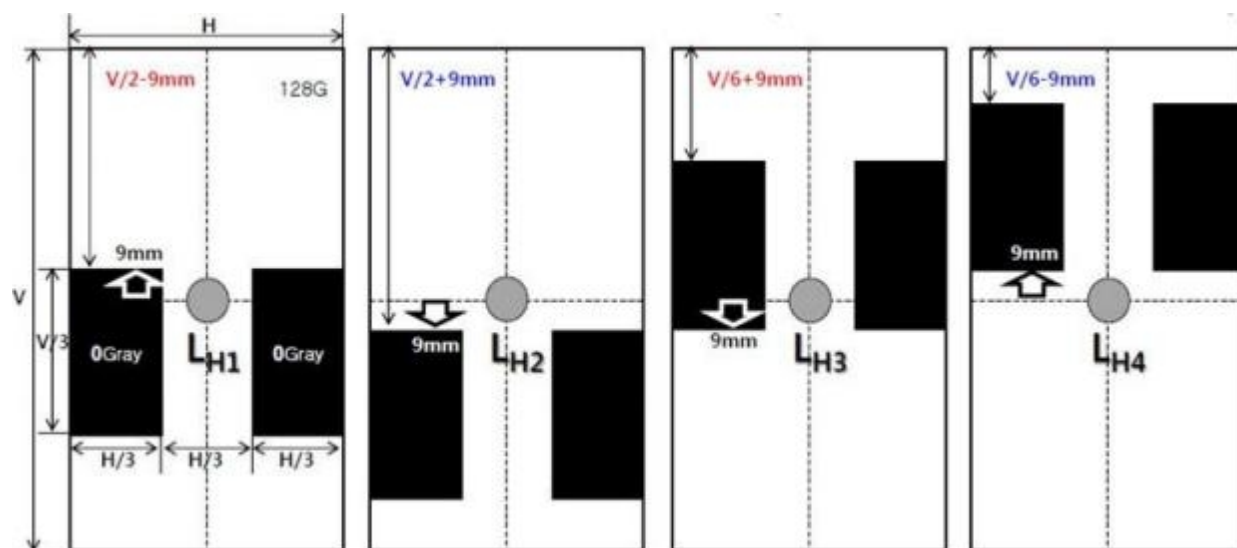
**Note5: Cross-talk**

22% black window , 128 gray background. Pattern Left/Right 9mm shift

$$\text{Crosstalk}(V) = \max\left(\left|\frac{L_{V1} - L_{V2}}{L_{V2}}\right| \times 100, \left|\frac{L_{V3} - L_{V4}}{L_{V4}}\right| \times 100\right)$$



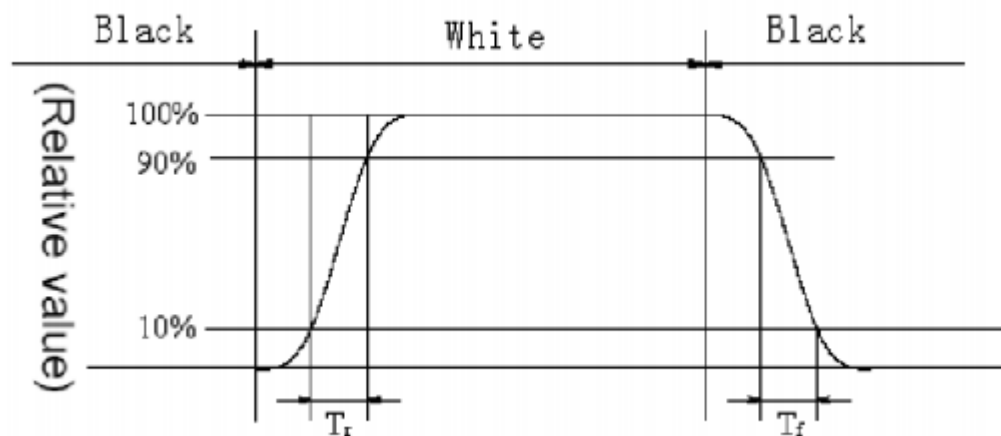
$$Crosstalk(H) = \max \left( \left| \frac{L_{H1} - L_{H2}}{L_{H2}} \right| \times 100, \left| \frac{L_{H3} - L_{H4}}{L_{H4}} \right| \times 100 \right)$$



**Note6: Response Time**

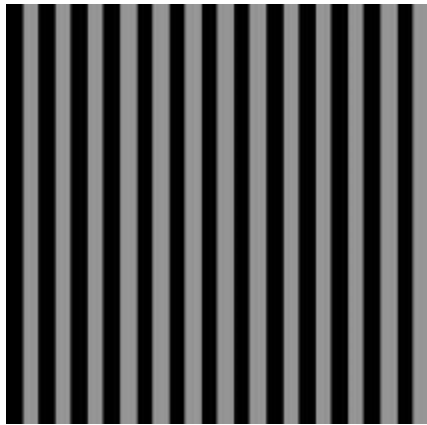
Response time=Pixel turn on and turn off time (White<=>Black).

It is measuring transition time from 10% to 90% of luminance.



**Note 7: Flicker**

Suggested Instruments: Konica Minolta CA-310 or Klein Instruments K-8



**Odd row : L0 Black**  
**Even row : L186 gray level**

**Flicker Test Pattern**

The flicker level is defined by Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20 \log_{10} \left( 2 \frac{f_{FFTc}(n)}{f_{FFTc}(0)} \right) + FS(Hz) \quad (dB)$$

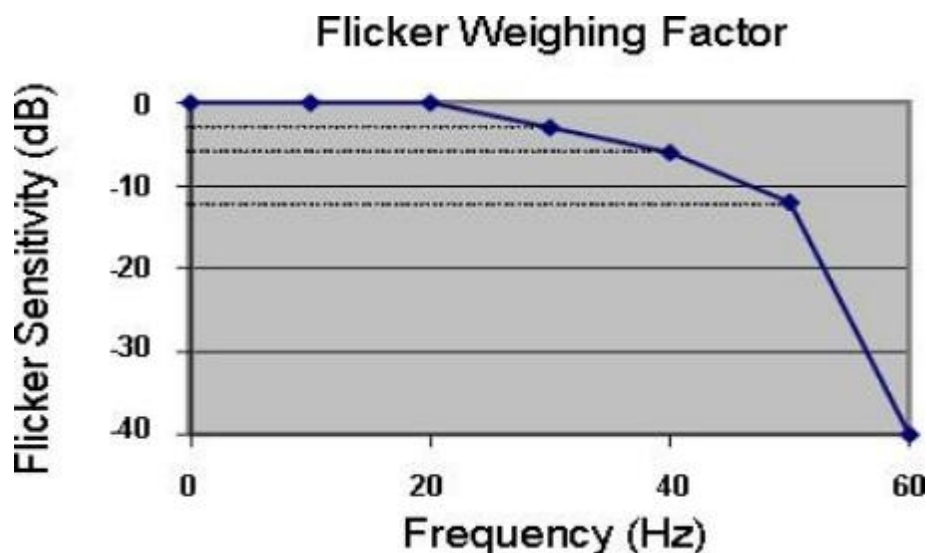
Where

$f_{FFTc}(n)$  is the n-th FFT coefficient.

$f_{FFTc}(0)$  is the 0-th FFT coefficient which is DC component.

$FS(Hz)$  is the flicker sensitivity as a function of frequency.

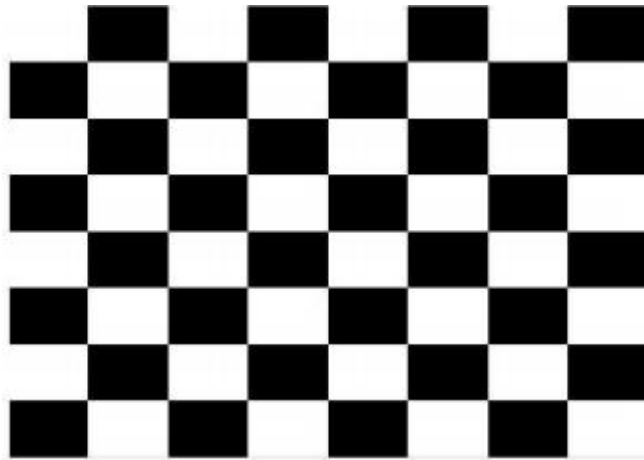
The peak flicker level shall be reported based on the calculation using above formula in which  $FS(Hz)$  is determined by the flicker weighing factor shown below.



**Note8: Image Retention**

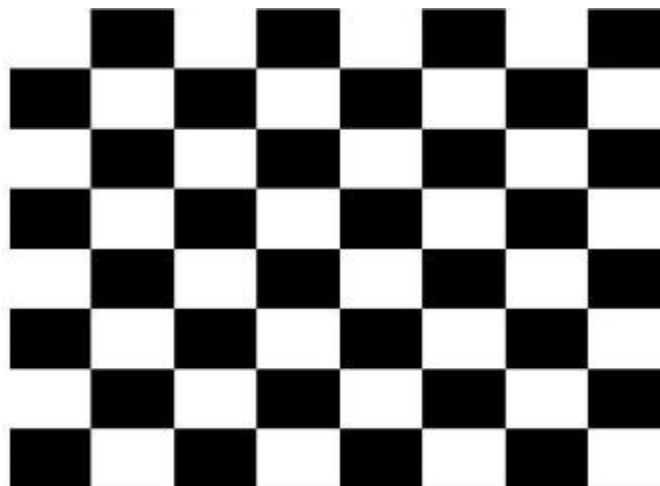
Using chessboard pattern (8 \* 8 ) light on 1hr, and switch to 127gray.

The Image retention should not be seen after 3 mins.

**Note9: Image Sticking**

Using chessboard pattern ( 8 \* 8 ) light on 3 hrs, and switch to 127 gray.

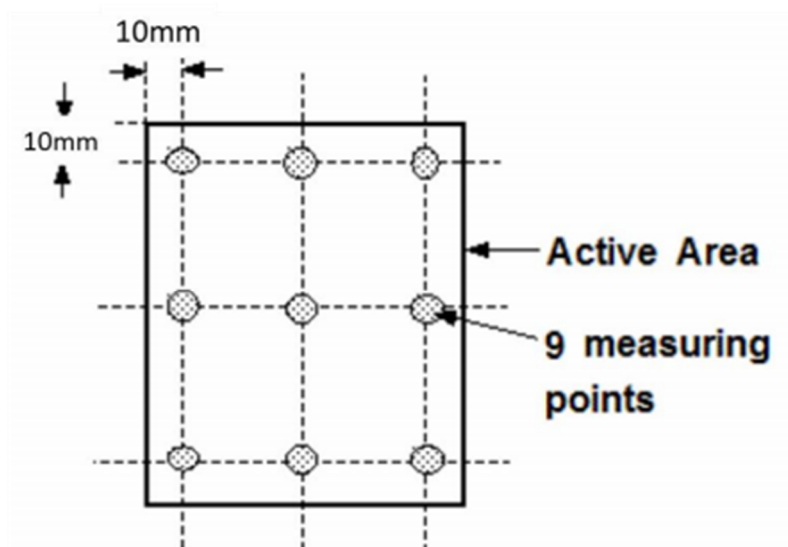
The Image Sticking should not be seen after 60 min with ND02 filter (image sticking disappear after stewing).



**Note10: Color Uniformity**

Total 9 measure points should set as shown in the following figures. The CIE 1967 Standards shall be used. The color difference is calculated by using following formula:

Max ( $\Delta u'v'$ ) (the max  $\Delta u'v'$  value between two random point of 9 point)



## 6 Reliability

### 6.1 Environmental Test

| No | Item                                               | Conditions              | Quantity | Note                                                                                                                                                                                                                                   |
|----|----------------------------------------------------|-------------------------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1  | High Temperature Operating (HTO)                   | 70 °C / 48hrs           | 5pcs     | After testing<br>- No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity test are permitted.<br>No function-related abnormalities. |
| 2  | Low Temperature Operating (LTO)                    | -20 °C / 48hrs          | 5pcs     |                                                                                                                                                                                                                                        |
| 3  | High Temperature Storage (HTS)                     | 80 °C / 48hrs           | 5pcs     |                                                                                                                                                                                                                                        |
| 4  | Low Temperature Storage (LTS)                      | -30 °C / 48hrs          | 5pcs     |                                                                                                                                                                                                                                        |
| 5  | High Temperature / High Humidity Operating (HTHHO) | 60 °C / 93%R.H. / 96hrs | 5pcs     |                                                                                                                                                                                                                                        |
| 6  | High Temperature / High Humidity Storage (HTHHS)   | 60 °C / 93%R H / 96hrs  | 5pcs     |                                                                                                                                                                                                                                        |

**6.2 Electrical Test**

| No | Item                             | Conditions       | Note                                                                                                                                                       |
|----|----------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1  | Air discharged<br>Criteria C     | $\pm 8\text{kV}$ | After testing<br>- Harddefectshouldnothappen.<br>- If it would be recovered to normalstate afterresetting, it would be judged as a good state. ( Class C ) |
| 2  | Contact discharged<br>Criteria C | $\pm 4\text{kV}$ |                                                                                                                                                            |

**6.3 Mechanical Test**

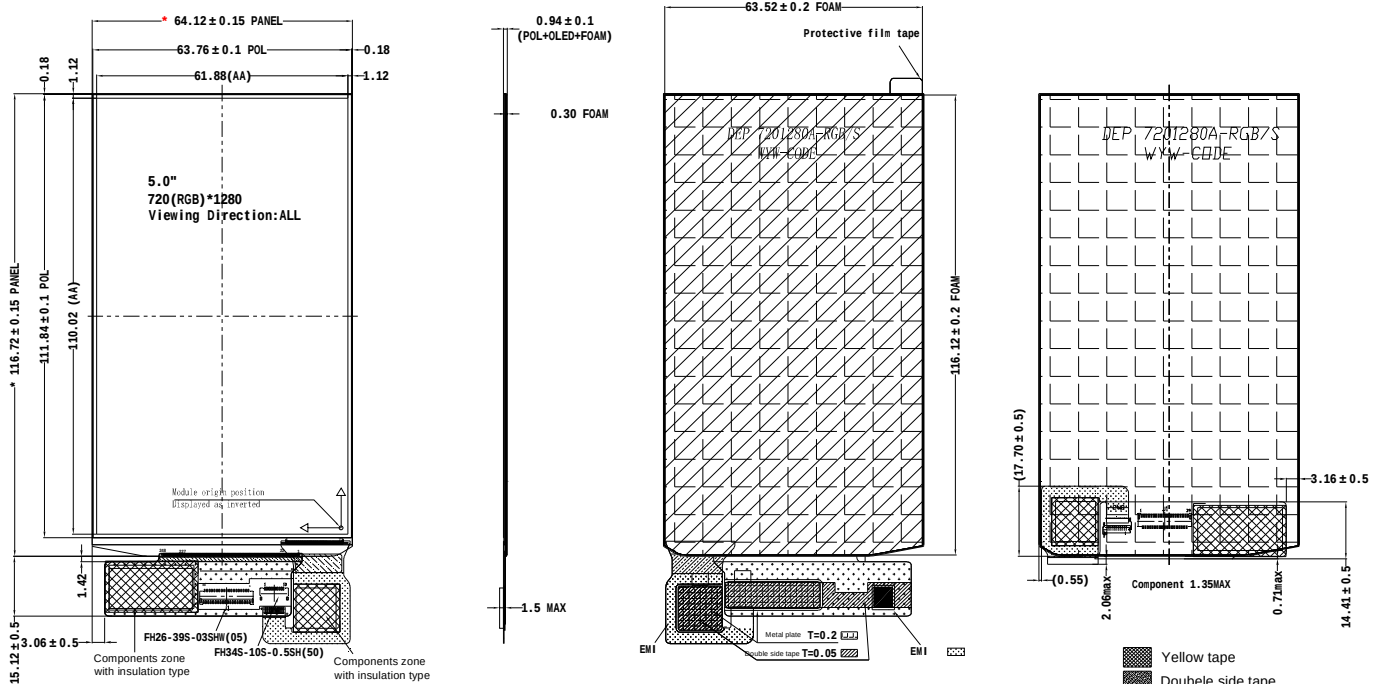
| No | Item                | Conditions                                                                                                                                                   | Note           |
|----|---------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 1  | Glass Strength Test | 4PB , B10 >100MPa (stress)                                                                                                                                   |                |
| 2  | BallDropTest        | 0.2J @ center<br>32g, 45cm                                                                                                                                   | Module with CG |
| 3  | Drop Test           | 10 Drops: 6 surfaces / 3edges / 1corner/ for Carton test & Gift Box Test<br>0~9kg /92cm<br>9.2kg~ 18.2kg /76cm<br>18.3kg~27.2kg /61cm<br>27.3kg~45.4kg /46cm | Package        |
| 4  | Vibration Test      | Accleration:1.48Grms<br>5~ 100Hz 0.015G*2/Hz /<br>100~200Hz -6dB/Oct/<br>200Hz 0.0038G*2/Hz /<br>Test Time : 30 min                                          | Package        |

## **7 Handling Precautions**

- 7.1 When cleaning ITOpad, avoid using hard and abrasive material or corrosive solution
- 7.2 Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity
- 7.3 Strong impact & pressure on module and packing is prohibited
- 7.4 Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display
- 7.5 Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available
- 7.6 Image sticking may occur if an image displays for an extended period of time
- 7.7 When interfered by system's overall mechanical design, an abnormal display may occur
- 7.8 After considering emitting energy, you should plan your design to satisfy EMI standards.
- 7.9 Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

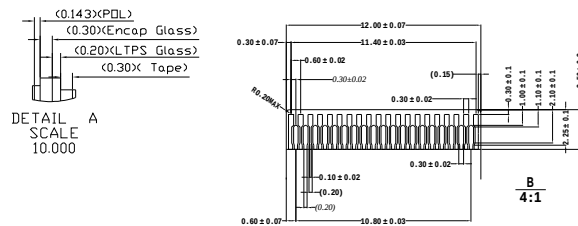


## 8 Outline Dimension Drawing



## NOTE:

- 1.DISPLAY TYPE: AMOLED 4.97'HD,16.7M COLORS
- 2.VIEWING DIRECTION: ALL
- 3.RESOLUTION RATIO: 720(RGB) X 1280 DOTS
- 4.DRIVER IC: RM67295
- 5.Interface: MIPI 4 lanes
- 6.OPERATING TEMP: -20 °C TO 70 °C  
STORAGE TEMP: -30 °C TO 80 °C
- 7.Tape \* is the key size
- 8.RoHS COMPLIANT.
- 9.It is recommended to reserve a gap of 0.3mm between the back of the module and the housing in the thickness direction.
- 10.It is recommended that the VA window be 0.3mm larger than the AA side of the module.



HRS FH26-39S-03SHW or equivalent

- Yellow tape
- Double side tape
- Conductive tape
- Single layer zone
- EMI film

| Pin | Name          |
|-----|---------------|
| 1   | GND           |
| 2   | VBAT          |
| 3   | VBAT          |
| 4   | VBAT          |
| 5   | VBAT          |
| 6   | VBAT          |
| 7   | GND           |
| 8   | GND           |
| 9   | GND           |
| 10  | MTP_PWR       |
| 11  | TE            |
| 12  | RESX          |
| 13  | VDDI(1.8V)    |
| 14  | GND           |
| 15  | D2P           |
| 16  | D2N           |
| 17  | GND           |
| 18  | D1P           |
| 19  | D1N           |
| 20  | GND           |
| 21  | CKP           |
| 22  | CKN           |
| 23  | GND           |
| 24  | D0P           |
| 25  | D0N           |
| 26  | GND           |
| 27  | D3P           |
| 28  | D3N           |
| 29  | GND           |
| 30  | VCI(3.3V)     |
| 31  | GND           |
| 32  | TP_VCC(2.8V)  |
| 33  | TP_VDDI(1.8V) |
| 34  | TP_INT        |
| 35  | TP_SDA        |
| 36  | TP_SCL        |
| 37  | TP_RESX       |
| 38  | NC            |
| 39  | GND           |